# USB Radio Interfaces

## Contents





## 1. Introduction

These are simple radio interfaces using combinations of CMedia CM108[3]I USB interface, usb hub SL2-1AL on page 27, CH340[2]K usb-serial convertor and transformer / opto isolation of the interface.

This manual collated in Latex. If you want to contribute more material contact Simon ZL1THH or Keith ZL1BQE

### 1.1. History

This project started as a simple interface for connection a radio to the internet for digital modes, and Echolink Winlink was not in mind during development.

The 1st version used surface mount devices and was the first project to use these parts it was also my first attempt at making the board fit in to a box that was readily available ( Jaycar part) it was also my first attempt at making front an back panels using PCB material and getting them made by JLCPCB

Of course it didn't fit first time the holes for the USB connector on the front was out by a few mm and everything was off be a few mm on the back panel I did not have the PCB far enough back in the box to allow the 3.5mm sockets to protrude through the panel

Lots of mistakes on the first attempt but was a good exercise in getting dimensions correct, I also didn't get the printing or solder resist on the right side of the front and back panels

2nd version was a lot better everything was in correct positions solder resist was black and screen printing on the correct side of the front and back panels

There were only 5 each of version 1 and 1.2 made

At this stage Papakura radio club had shown interest in this as a club project but didn't like the surface mount version it was then changed to Through hole parts (v1.3) with the exception of the USB hub and USB to serial devices they are not available as through hole parts

The interface used the 3.5mm or 6 pin Mini DIN to connect to the radio The Mini DIN plug is a bit difficult to connect so the PCB was changed (v1.5) to an RJ45 at the same time I changed the 10uF and 1uF electrolytics to multilayer type non polar capacitors there was also a few track changes around the MAX232 device

## 2. USB Radio Interfaces

This has one audio channel [3] and a usb-serial interface [2] and built in USB Hub . There have been three versions. The interface pinout is shown in appendix B on page 14 and drivers can be downloaded from [1]


Figure 1: V1 Interface


Figure 2: V1.5 Interface

## 2.1. V1.5 RJ-45

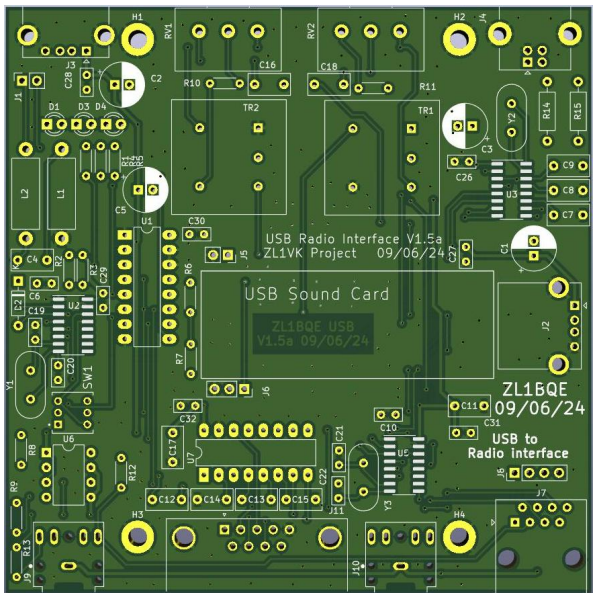



Figure 3: PCB

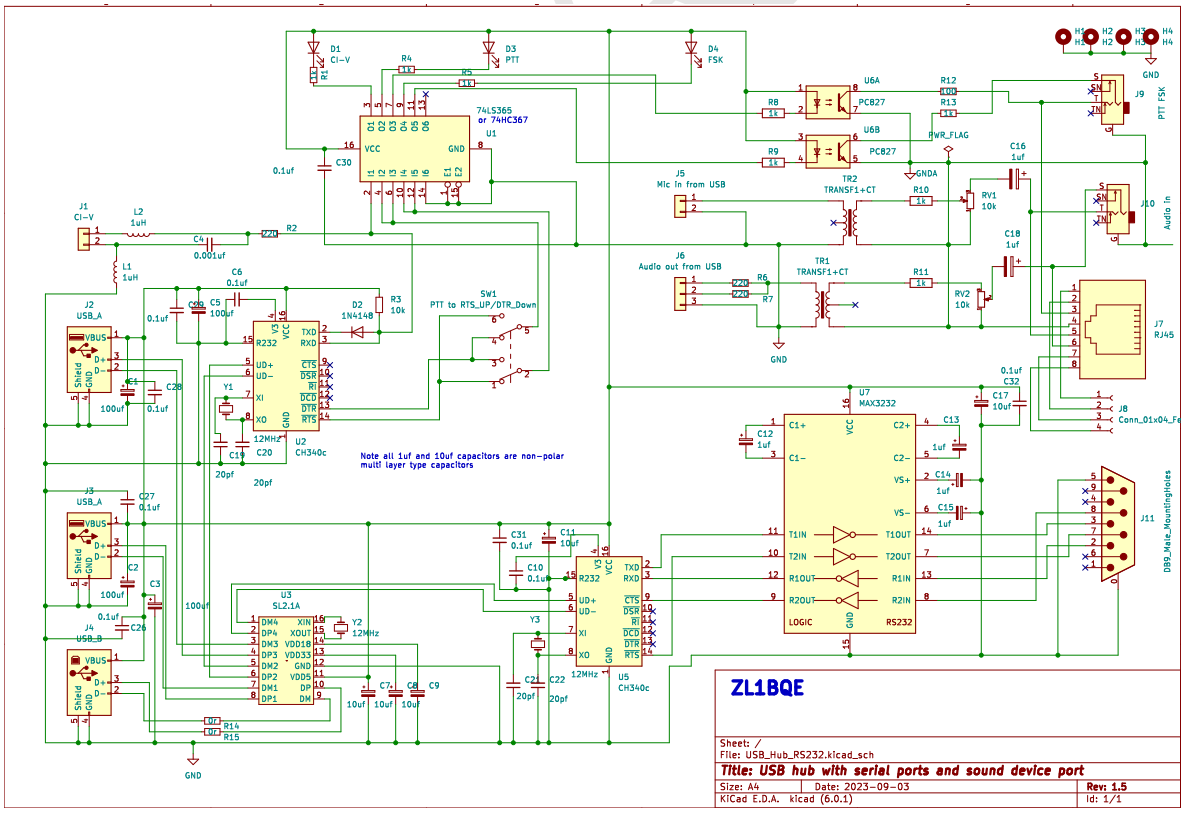



Figure 4: Schematic (A)

## 2.2. V1.3 Mini DIN, Through hole.

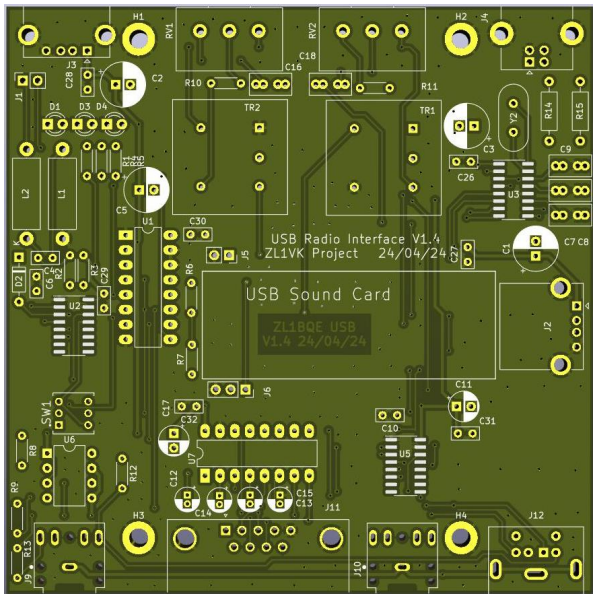



Figure 5: PCB

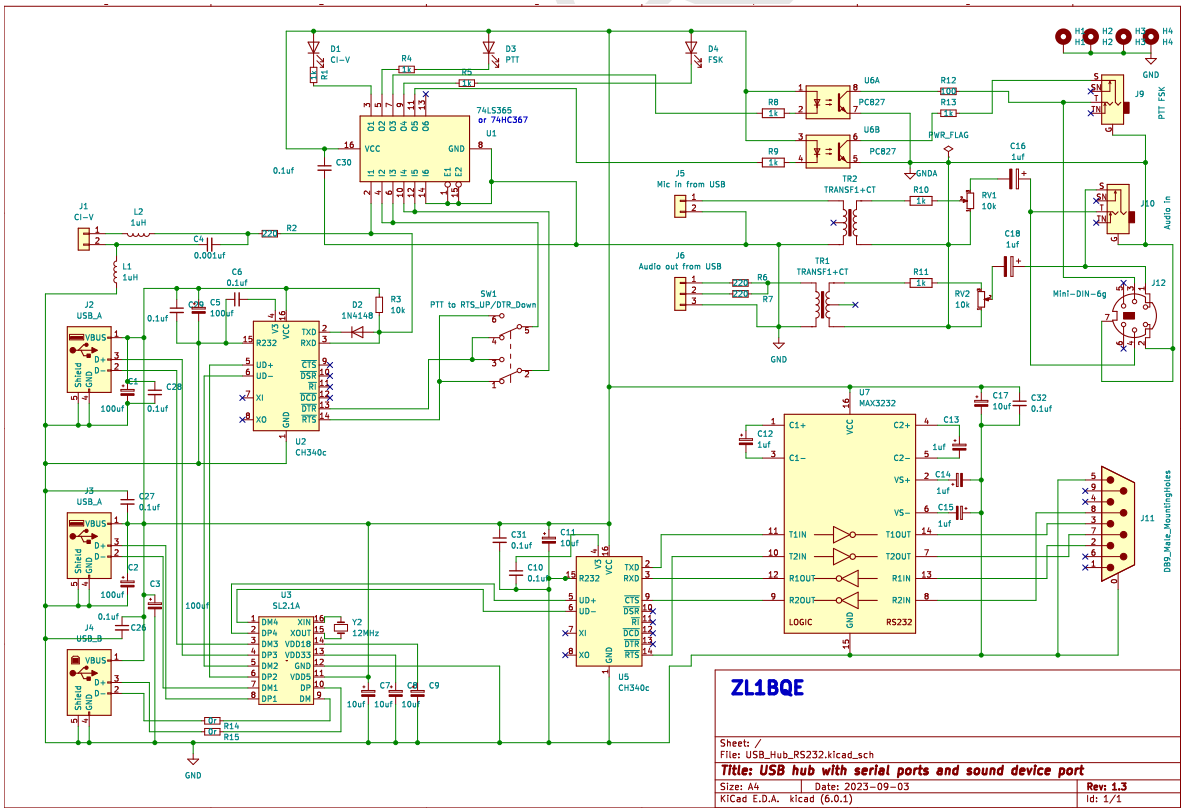



Figure 6: Schematic (A)

## 2.3. V1 SMD

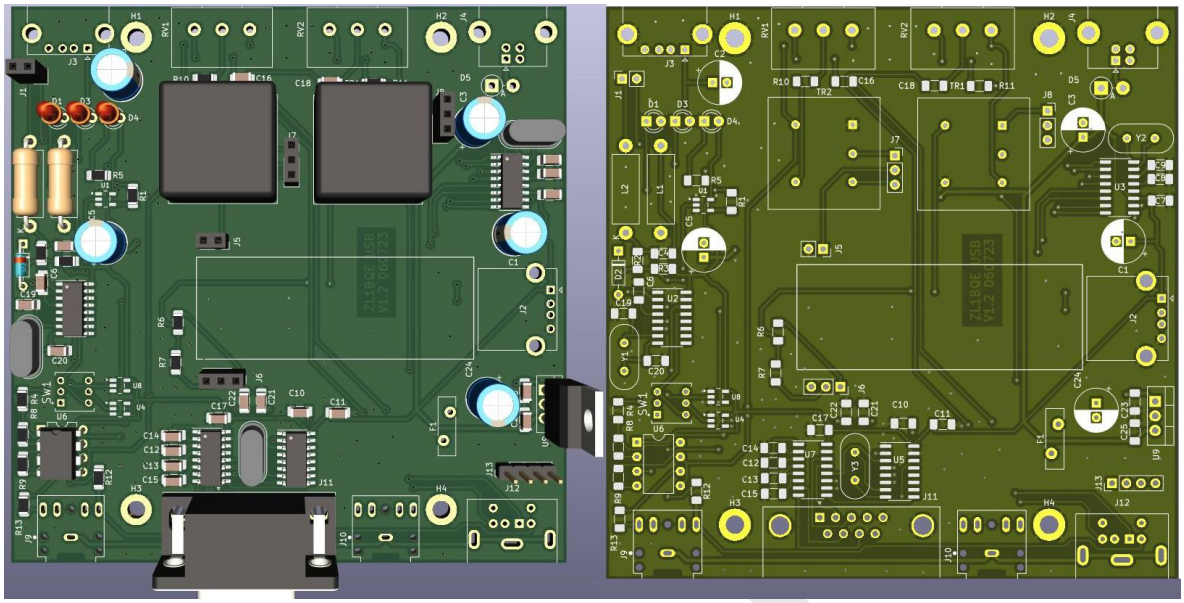


Figure 7: PCB

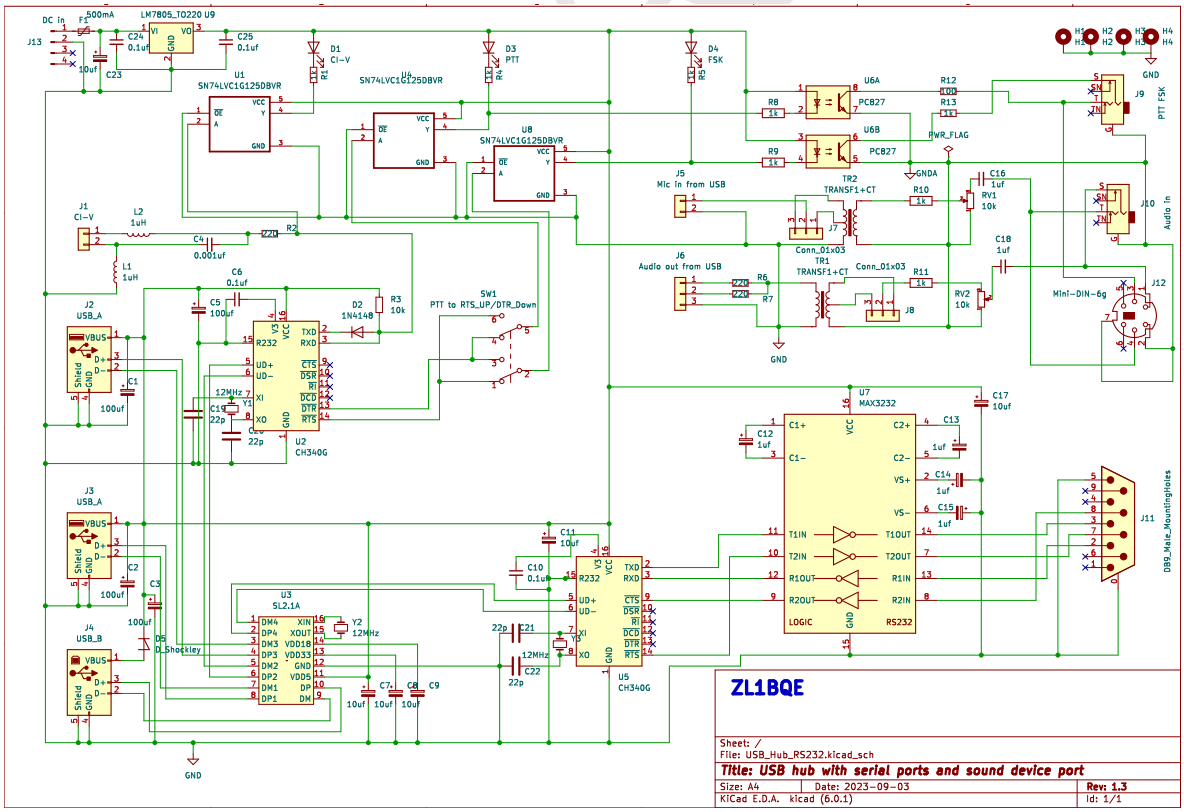



Figure 8: Schematic (C)


Figure 9: V1 Assembled PCB

# 3. CM119 Winlink interface

This board was developed as an alternate to using the USB sound cards it uses a CM119A[4] J on page 23 device which is similar to the CM108 used on the USB sound cards.

There are several General Purpose Input/output pins available on this part ZL1SWW mentioned they could be used for another type of interface


Figure 10: CM119 Interface

## 3.1. V1

This was my first attempt at using the 48 pin QFP devices the pin spacing is a challenge when soldering without the proper equipment. I also fitted a USB socket for the PC connection this was also a challenge to solder

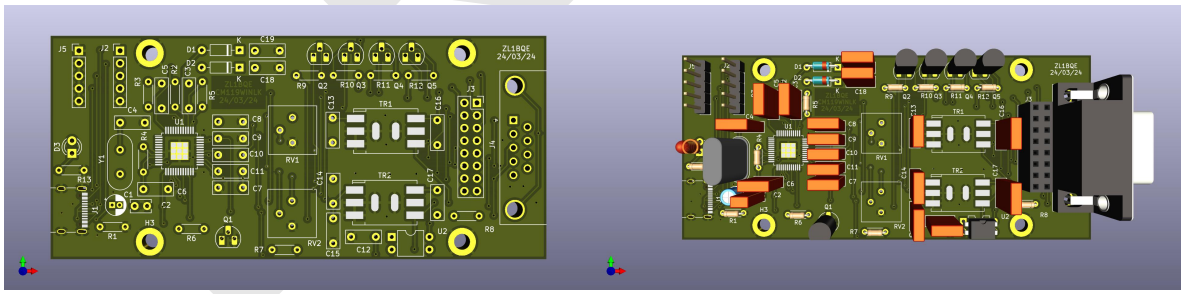


Figure 11: CM119 V1 PCB

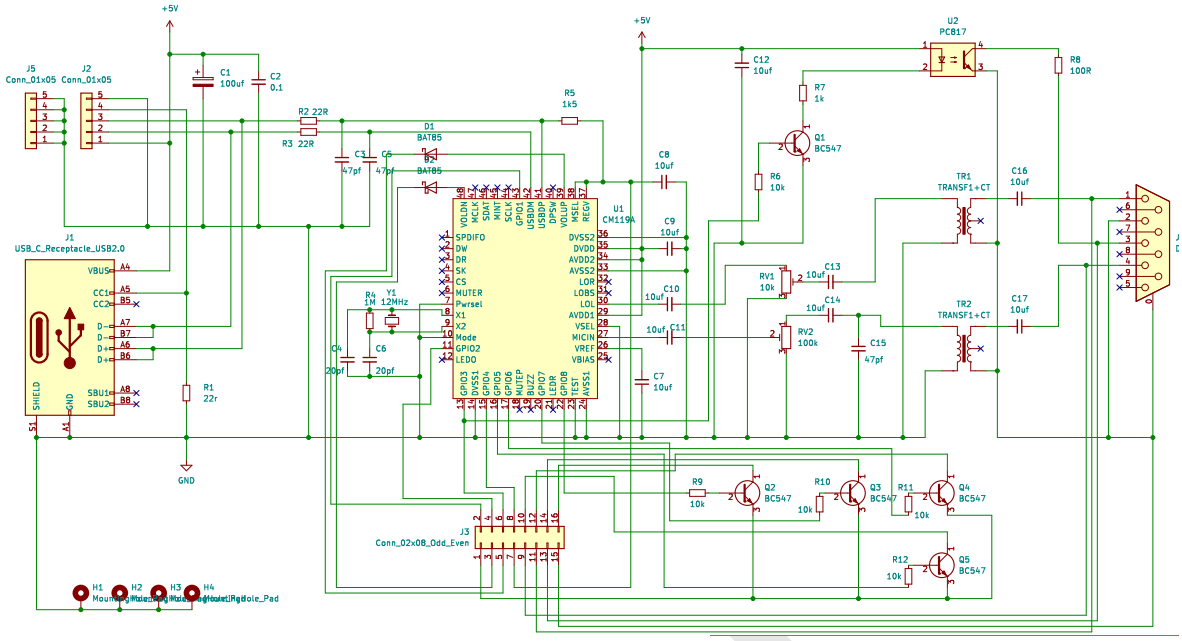



Figure 12: CM119 V1 Schematic (A on page 19)

## 3.2. V2

This is a smaller version of the V1 and made to fit into a small aluminium box a TX led and USB activity LED were added to give an indication of operation. An adapter board fitted with a USB C socket was used for the computer connection.

A small 50mm by 20mm PCB front panel was made to fit the end of the box one with the option of a 3.5mm jack as the connections to the radio the other had a DB9 socked on the other end of the PCB.

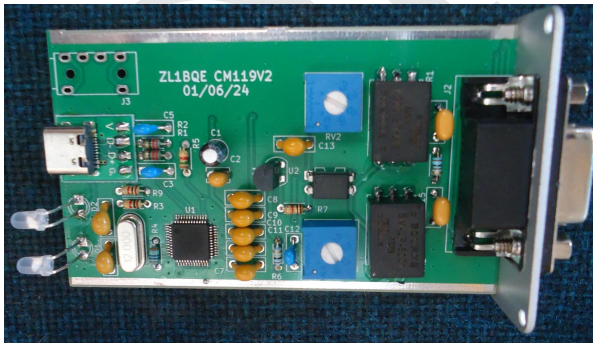



Figure 13: CM119 V2 Assembled PCB

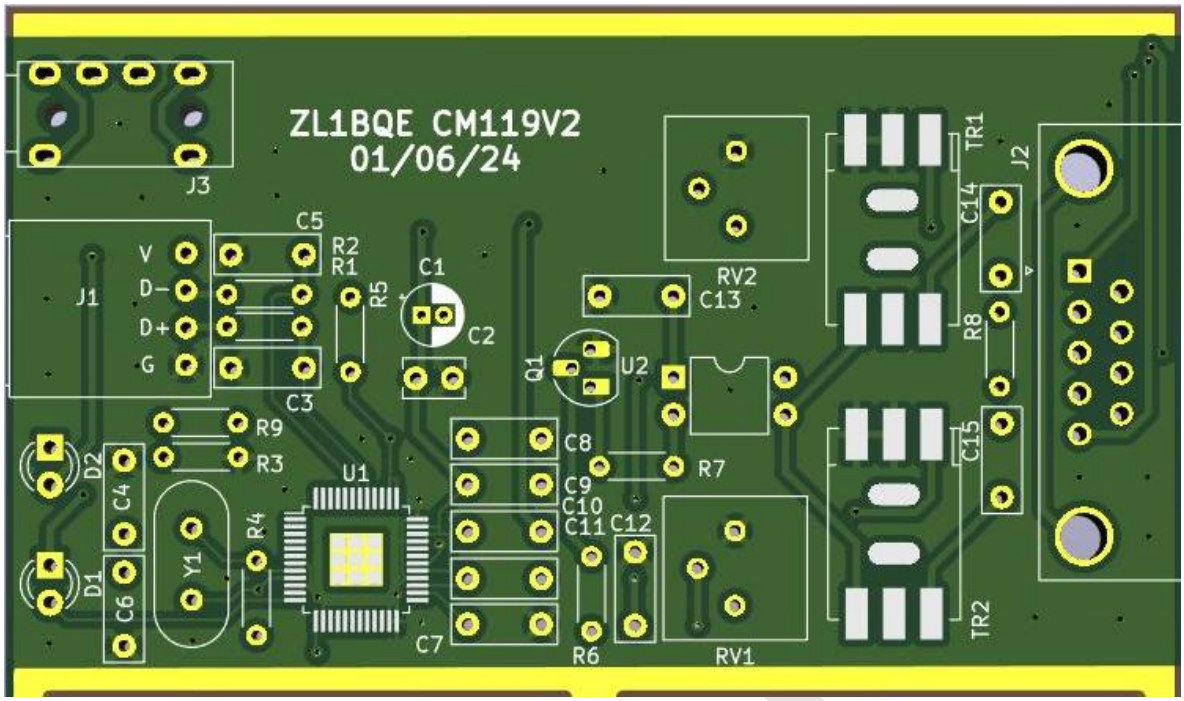



Figure 14: CM119 V2 PCB

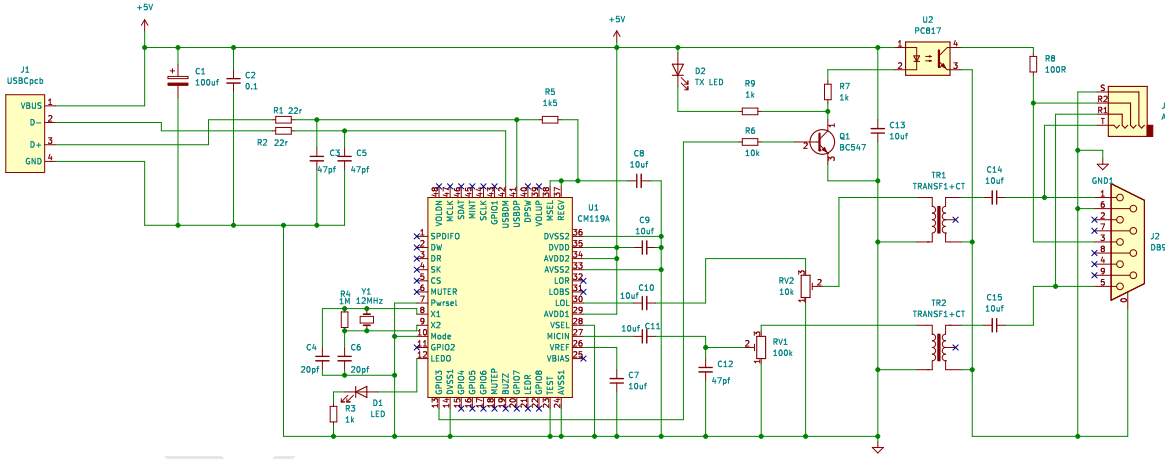



Figure 15: CM119 V2 Schematic (A)

## 4. Dual Radio Interface

This is made to combine a 2m and 70cm radio into a single Winlink node. It has dual Cm108 USB audio I on page 21 and a CoreChips SL2-1A USB hubL on page 27, but no serial interface, as it is designed for pre-programmed channelised radios.


Figure 16: Dual Radio Interface

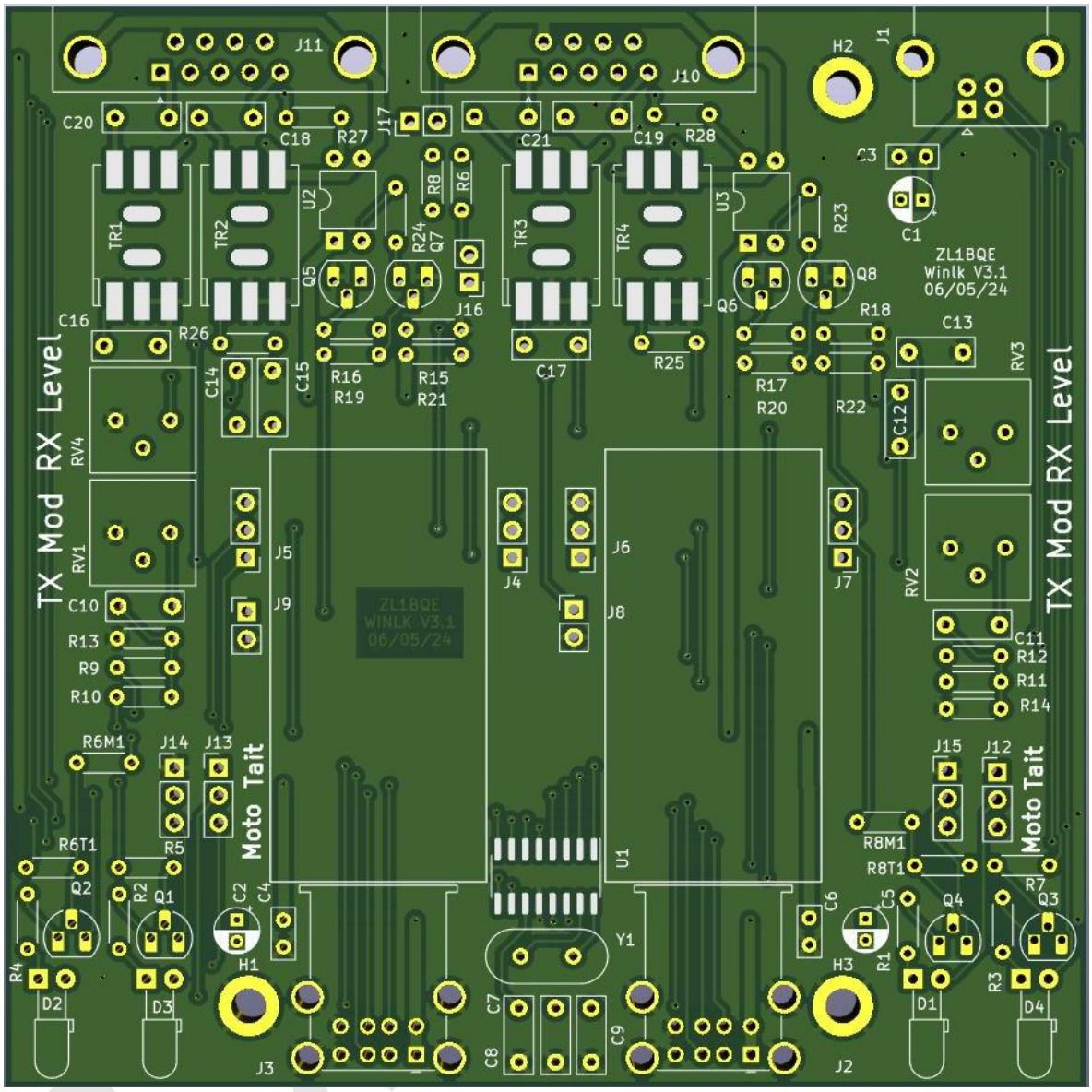



Figure 17: Dual Interface PCB

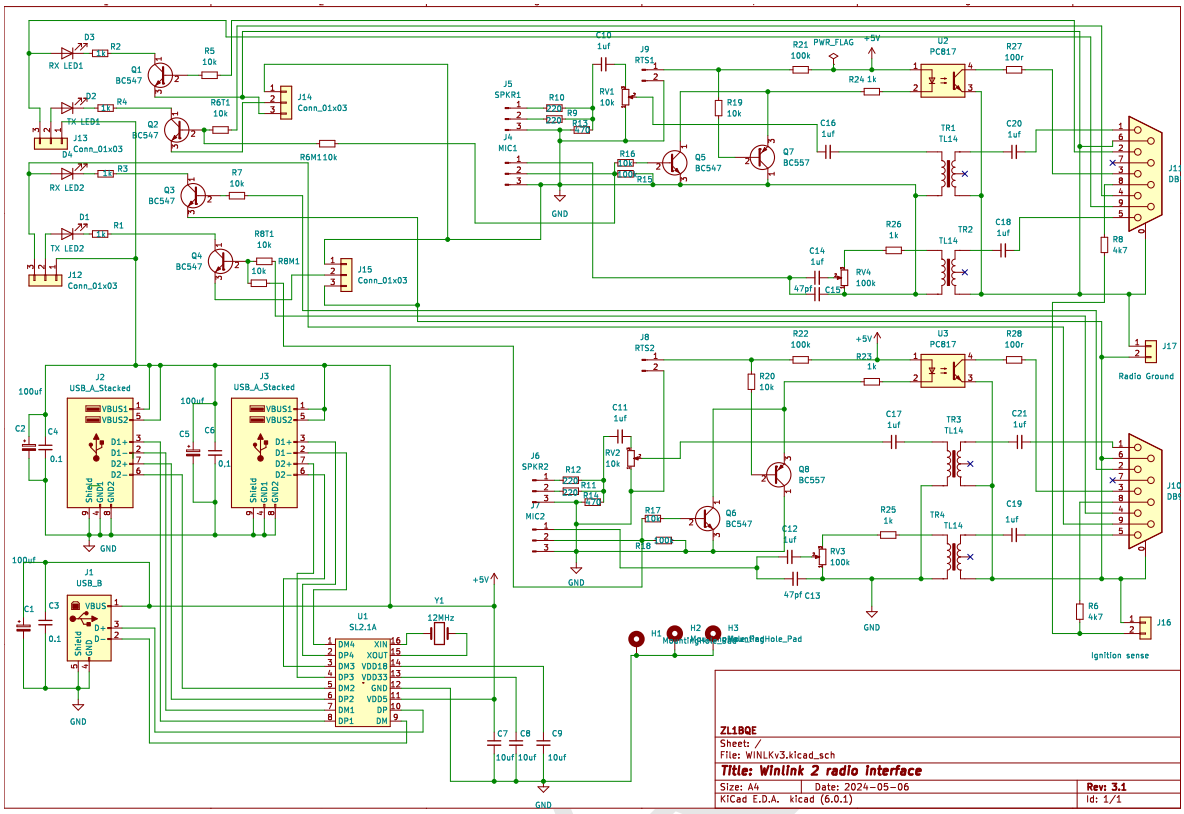



Figure 18: Dual Interface Schematic (H)

## References

[1] Install CH340 drivers from Arduino CH340 Driver Download

[2] CH340 Product Page K on page 25

[3] CMedia CM108 CMedia CM119CMedia CM119 I on page 21

[4] CMedia CM119 https://www.cmedia.com.tw/products/USB20_FULL_SPEED/CM119B J on page 23

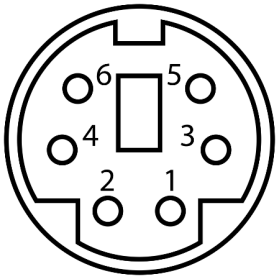
[5] CoreChips Sl2-1A USB Hub L

## A. Revision History

| Rev | Date | Changes |
|---|---|---|
| 0 | 16 July 2024 | Draft Release |
| 1 | 18 July | Add photos, CM119 datasheet, webpage links to sections |
| 2 | 19 July | Reduce photo resolution to shrink pdf |
| 3 | | Change link colors |

# B. Interface Pinouts

Mini Din connector on back of interface




Pin 2 Ground

Pin 1 Audio out (connect to audio in of the radio)

Pin 3 PTT ( active Low)

Pin 4 Audio input (connect to audio out from radio)

RJ45 connector

| | |
|---|---|
| 1 | Not used |
| 2 | not used |
| 3 | PTT Active low |
| 4 | Ground |
| 5 | Audio out connect to mic or line input on Radio |
| 6 | Audio input connect to speaker or line output on Radio |
| 7 | Not used |
| 8 | Not used |

Audio 3.5mm Jack

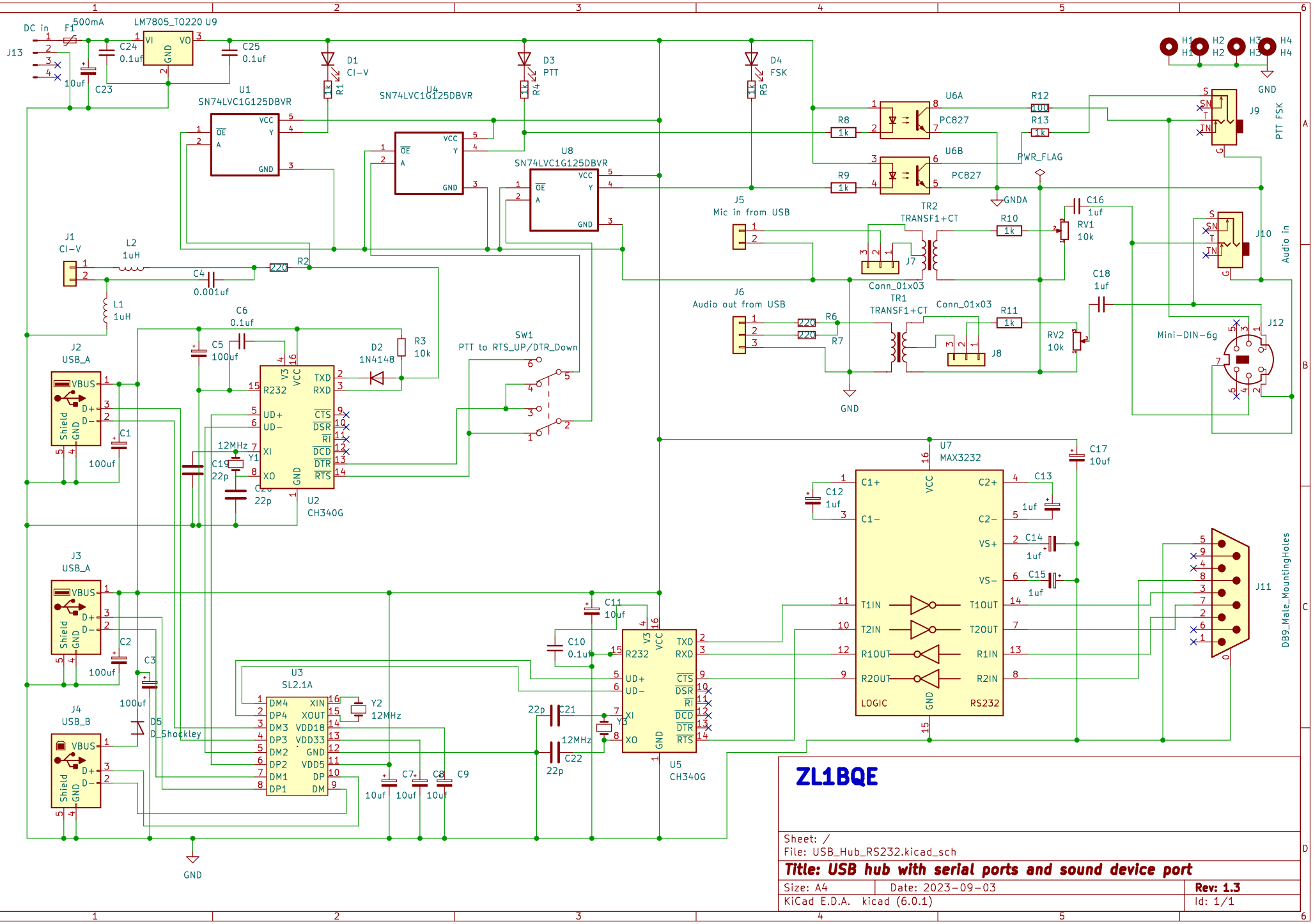
Tip is audio input

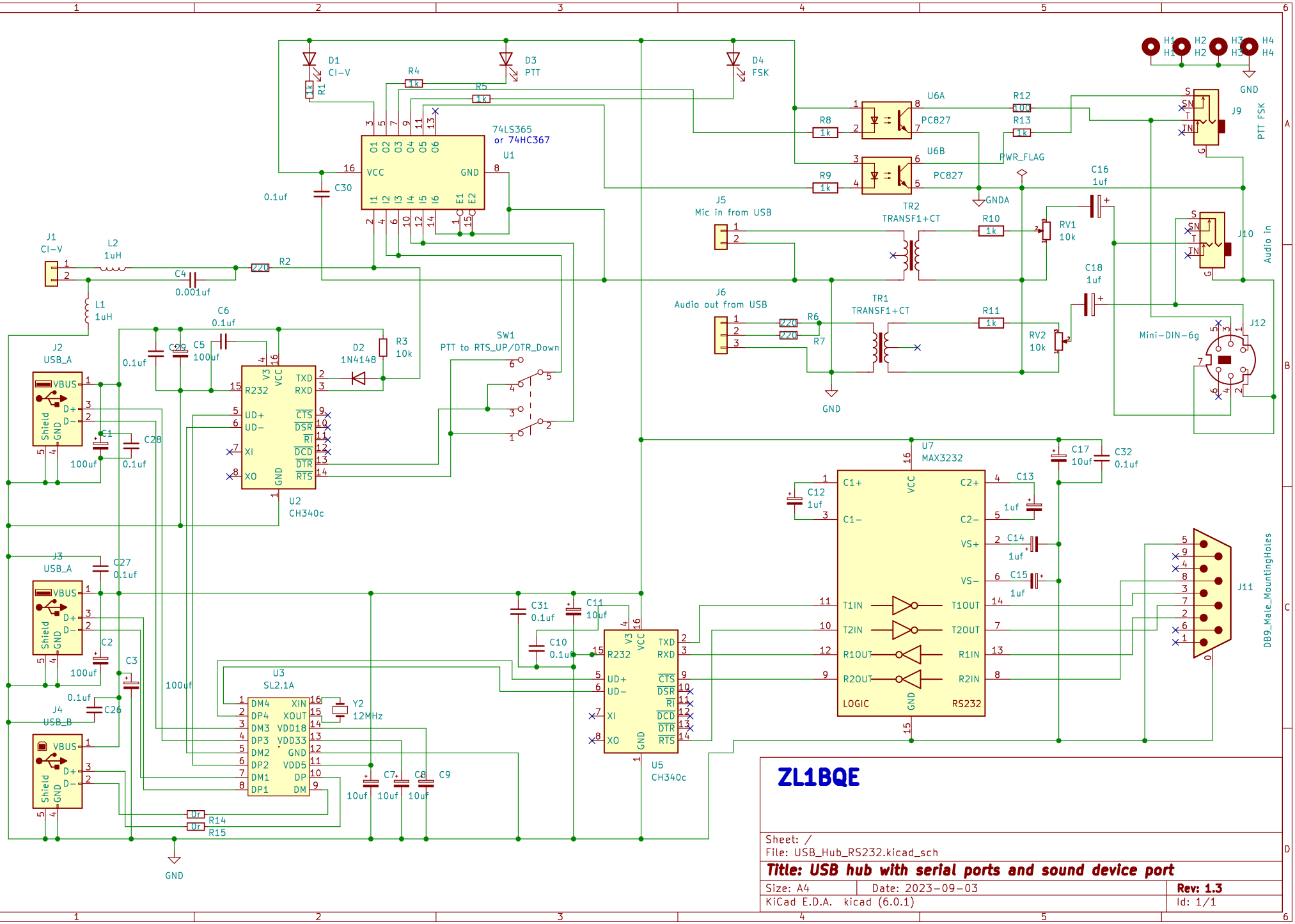
Sleeve is Audio out

FSK/PTT 3.5mm

Tip is PTT

Sleeve is FSK

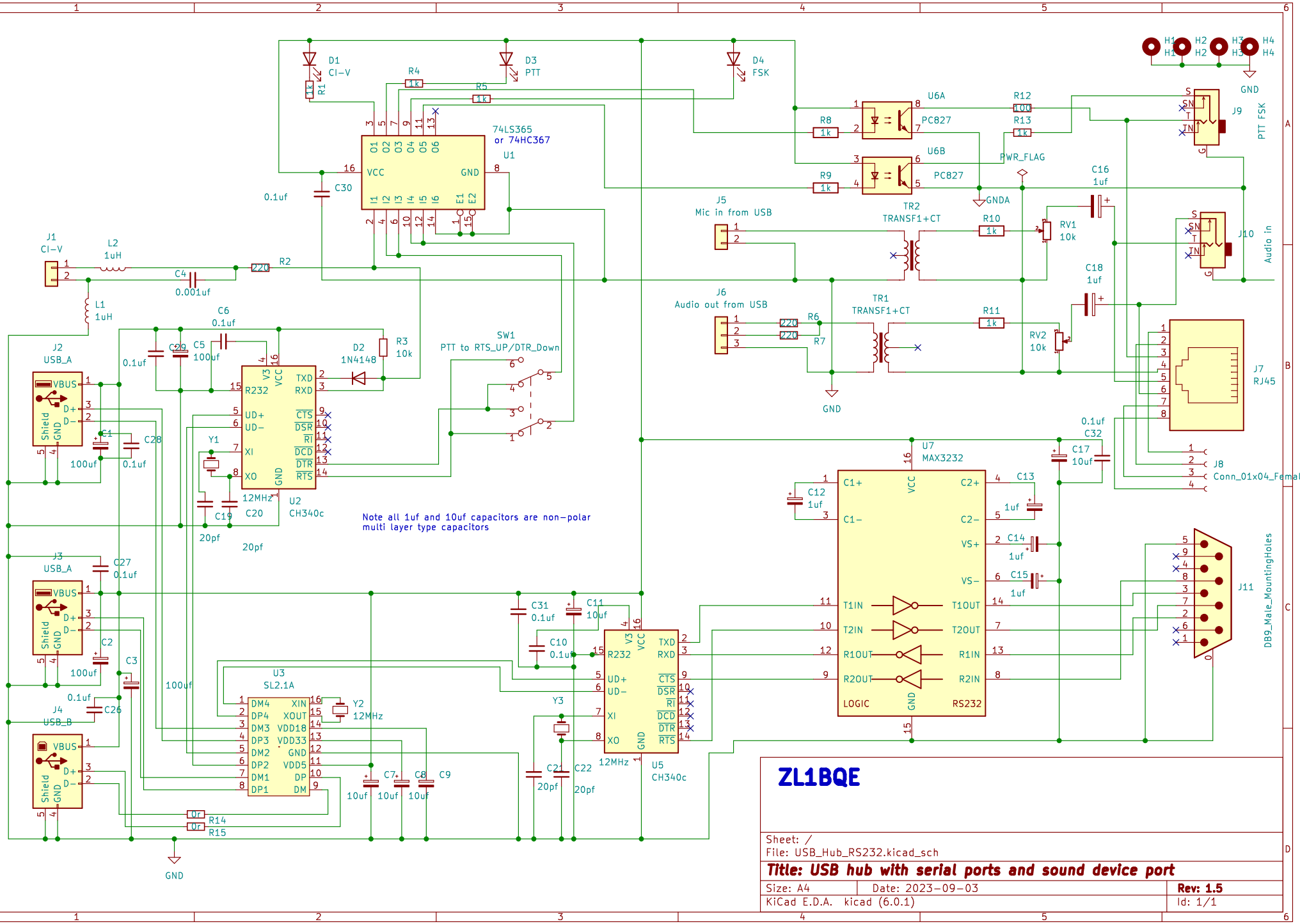

DC in
J13
F1
500mA
LM7805_TO220 U9
C24
0.1uf
C25
0.1uf
C23
10uf
D1
CI-V
R1
1k
D3
PTT
R4
1k
D4
FSK
R5
1k
U1
SN74LVC1G125DBVR
U4
SN74LVC1G125DBVR
U8
SN74LVC1G125DBVR
U6A
PC827
U6B
PC827
R8
1k
R9
1k
R12
100
R13
1k
PWR_FLAG
GNDA
J9
PTT FSK
J10
Audio in
J1
CI-V
L2
1uH
L1
1uH
C4
0.001uf
R2
220
J5
Mic in from USB
TR2
TRANSF1+CT
J7
Conn_01x03
R10
1k
C16
1uf
RV1
10k
C18
1uf
J6
Audio out from USB
R6
220
R7
220
TR1
TRANSF1+CT
Conn_01x03
J8
R11
1k
RV2
10k
J12
Mini-DIN-6g
C6
0.1uf
C5
100uf
D2
1N4148
R3
10k
SW1
PTT to RTS_UP/DTR_Down
J2
USB_A
C1
100uf
12MHz
C19
22p
Y1
C20
22p
U2
CH340G
U7
MAX3232
C17
10uf
C12
1uf
C13
1uf
C14
1uf
C15
1uf
J11
DB9_Male_MountingHoles
J3
USB_A
C2
100uf
C3
100uf
D5
D_Shockley
J4
USB_B
U3
SL2.1A
Y2
12MHz
C11
10uf
C10
0.1uf
22p
C21
12MHz
C22
22p
U5
CH340G
C7
10uf
C8
10uf
C9
10uf
GND
ZL1BQE
Sheet: /
File: USB_Hub_RS232.kicad_sch
Title: USB hub with serial ports and sound device port
Size: A4
Date: 2023-09-03
Rev: 1.3
KiCad E.D.A. kicad (6.0.1)
Id: 1/1
C. V1 Full Schematic



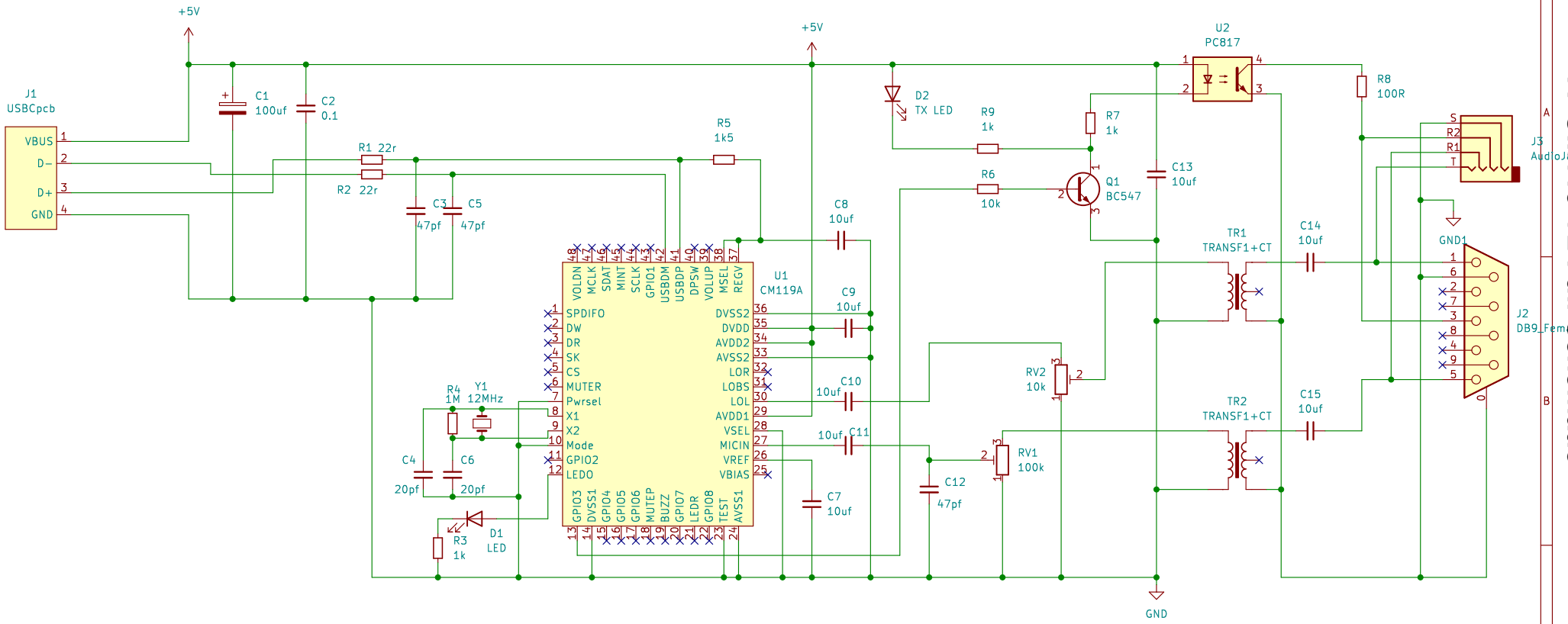

**ZL1BQE**

| | | |
|---|---|---|
| Sheet: / | | |
| File: USB_Hub_RS232.kicad_sch | | |
| **Title: USB hub with serial ports and sound device port** | | |
| Size: A4 | Date: 2023-09-03 | **Rev: 1.3** |
| KiCad E.D.A. kicad (6.0.1) | | Id: 1/1 |

**D. V1.3 Full Schematic**




E. V1.5 Full Schematic




# ZL1BQE

**ZL1BQE**

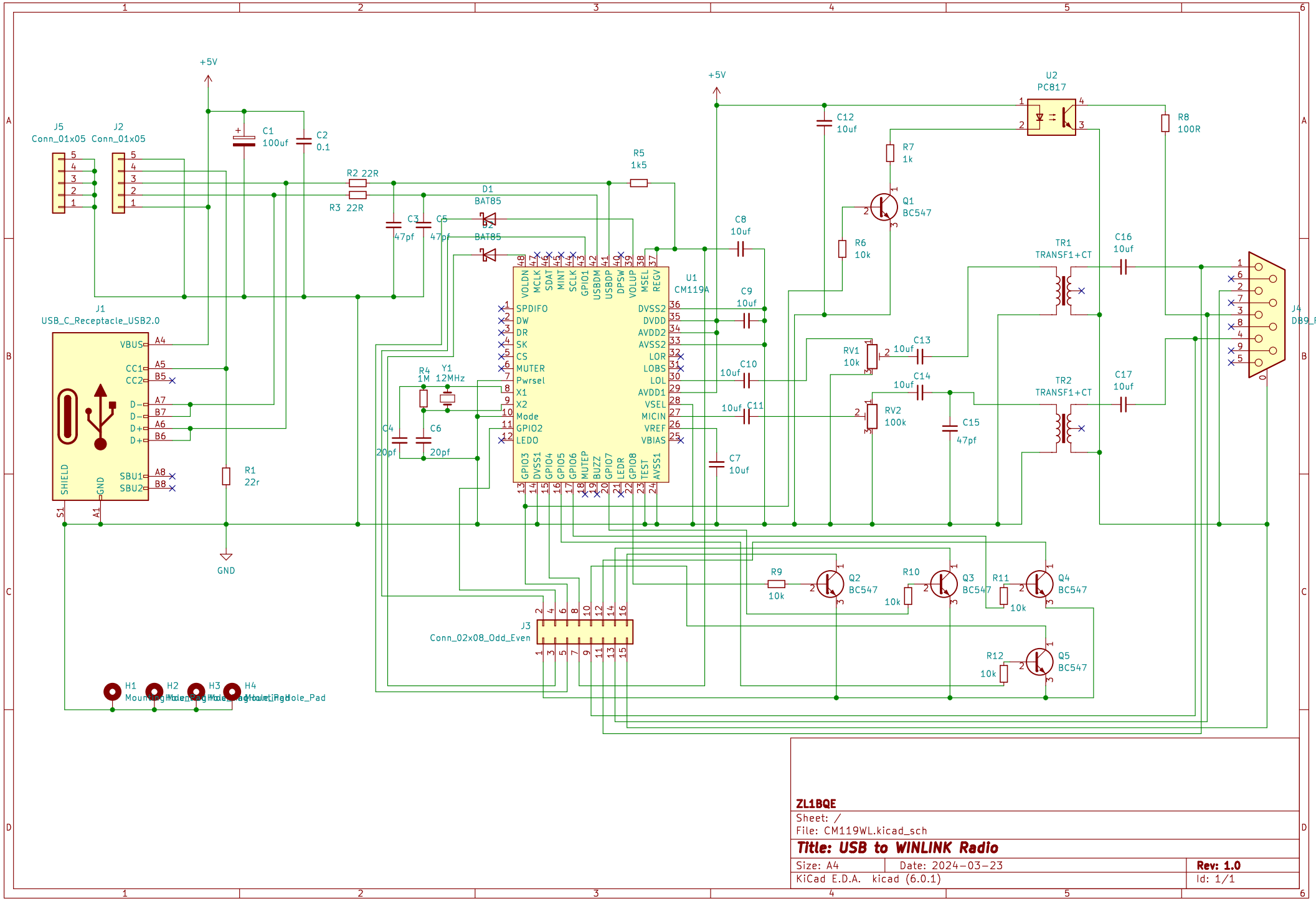
Sheet: /

File: CM119WLV2.kicad_sch

***Title: Winlink Radio iterface***

| Size: A4 | Date: | **Rev: 2.1** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.1) | | Id: 1/1 |

**F. CM119 V2 Full Schematic**




G. CM119 V1 Full Schematic

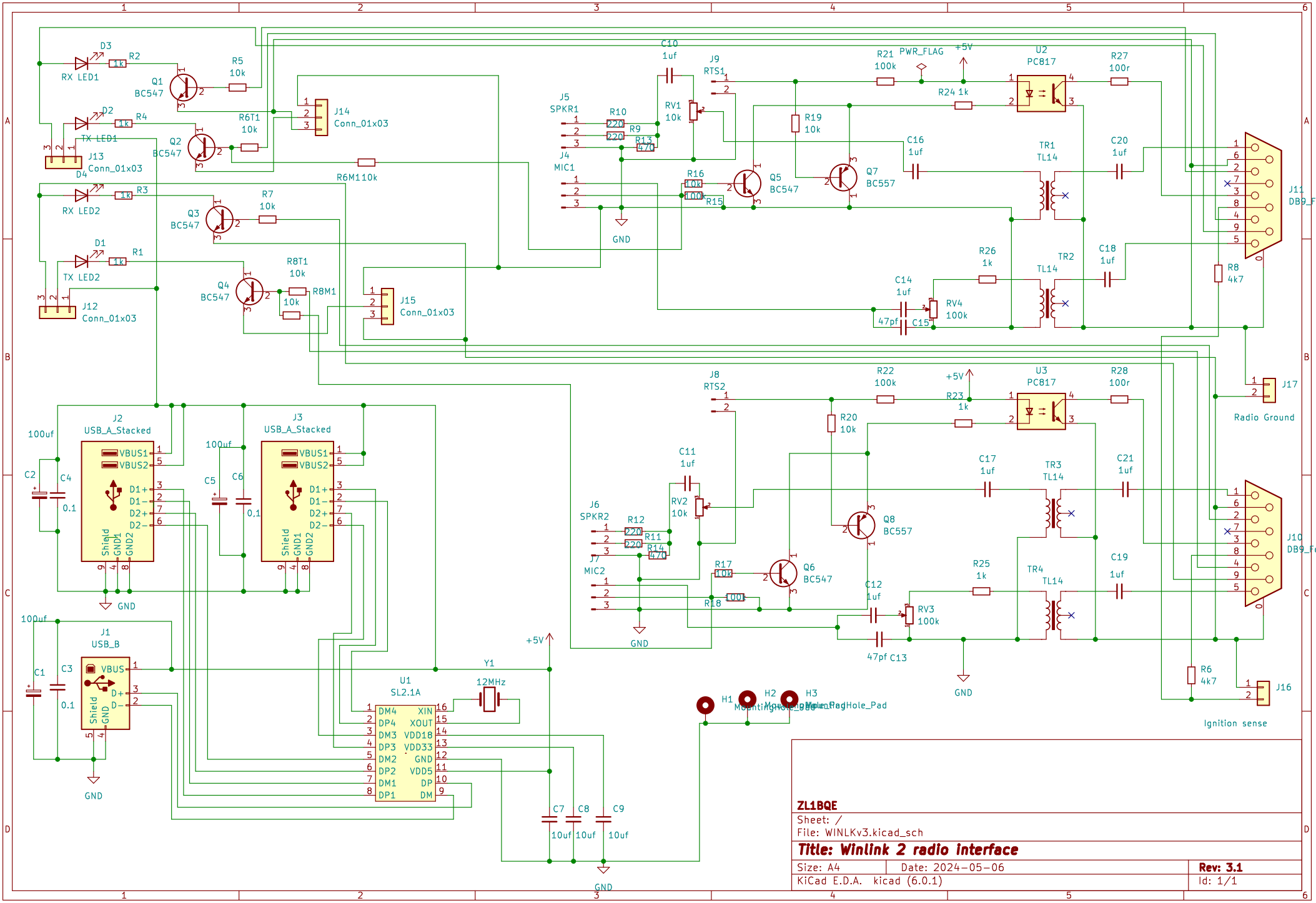
ZL1BQE

Sheet: /

File: CM119WL.kicad_sch

**Title: USB to WINLINK Radio**

| Size: A4 | Date: 2024-03-23 | **Rev: 1.0** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.1) | | Id: 1/1 |


H. Dual Interface Full Schematic
ZL1BQE
Sheet: /
File: WINLKv3.kicad_sch
Title: Winlink 2 radio interface
Size: A4
Date: 2024-05-06
Rev: 3.1
KiCad E.D.A. kicad (6.0.1)
Id: 1/1
Radio Ground
Ignition sense
GND
+5V
PWR_FLAG
RX LED1
TX LED1
RX LED2
TX LED2
Q1 BC547
Q2 BC547
Q3 BC547
Q4 BC547
Q5 BC547
Q6 BC547
Q7 BC557
Q8 BC557
U1 SL2.1A
U2 PC817
U3 PC817
J1 USB_B
J2 USB_A_Stacked
J3 USB_A_Stacked
J4 MIC1
J5 SPKR1
J6 SPKR2
J7 MIC2
J8 RTS2
J9 RTS1
J10 DB9_Female_Mo
J11 DB9_Female_Mo
J12 Conn_01x03
J13 Conn_01x03
J14 Conn_01x03
J15 Conn_01x03
J16
J17
TR1 TL14
TR2 TL14
TR3 TL14
TR4 TL14
Y1 12MHz
MountingHole_Pad

# I. CM108 Datasheet



**A Highly Integrated USB Audio Single Chip**

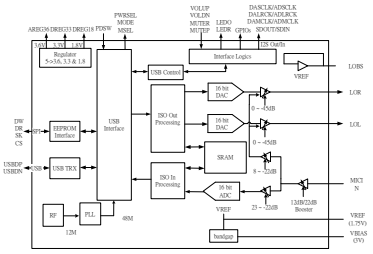
## DESCRIPTION

The CM108B is a highly integrated crystal-free USB audio single chip solution optimized for USB headset, headphone, and dongle applications. The CM108B comes with software driver interface which supports Xear™ sound effects for multimedia entertainments. All essential analog modules are embedded in the CM108B, including dual DAC and earphone driver, ADC, microphone booster, PLL, regulator and USB transceiver modules. Many features are programmable with jumper pins or by external EEPROM. Audio adjustments are easily controlled via specific HID-compliant volume control pins. An external codec or audio DSP can be connected to the CM108B via I2S pin for further processing. Vendors can customize unique USB VID/PID/Product String/Manufacture String and min/max/initial volumes to EEPROM. The CM108B also comes with an anti-pop noise circuits design and internal oscillator which can operate without an external crystal oscillator.

## FEATURES

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB Audio Device Class Specification v1.0
- Supports USB Suspend/Resume Mode and Remote Wakeup with Volume Control pins
- On-chip oscillator that provides reference sources for PLL and embedded USB transceiver
- Jumper pin for Headset Mode (Playback + Recording) and Speaker/Headphone Mode (Playback Only)
- Jumper pin for Mixer Unit enable/disable under Headset Mode and Power Mode setting
- I2S interfaces for external CODEC
- Anti-pop noise design for plugged and vice-versa
- Support Xear™ Audio Centre Software Driver for Windows OS

## BLOCK DIAGRAM









## 1 Description and overview

The CM108B is a highly integrated single-chip USB audio solution. All essential analog modules are embedded in the CM108B, including dual DAC and earphone driver, ADC, microphone booster, PLL, regulator and USB transceiver modules. It is perfectly suited to USB headset, USB earphone or USB audio-interface box applications. As well, many features are programmable with jumper pins or by external EEPROM.

The CM108B can connect to an external codec or audio DSP via I2S pins for further processing. Plus, 3 GPIO pins can be accessed with customer application software for additional value-adding applications. In addition, audio adjustments can be easily controlled via specific HID compliant volume control pins. Many features are programmable with jumper pins or external EEPROM. Vendors can customize unique USB VID/PID/Product String/Manufacture String and max/min/initial volumes to EEPROM. The CM108B also comes with an anti-pop noise circuits design and internal oscillator which can operate without an external crystal oscillator.

## 2 Ordering information

| Model No. | Package | Operating Ambient Temperature | Supply Range |
|---|---|---|---|
| CM108B | 48-pin LQFP, 7mm × 7mm × 1.4mm (plastic) | -20˚C to +70˚C | DVdd = 5V, AVdd = 5V |

## 3 Features

- Supports USB 2.0 full speed operation
- Compliant with USB audio device class specification 1.0
- Supports USB suspend/resume modes and remote wakeup with volume control pins
- On-chip oscillator that provides reference sources for PLL and embedded USB transceiver
- Support Xear™ audio driver for multimedia sound effects in Windows OS, for further information please refer to CM108B Xear™ Audio Center Driver User's Manual
- Jumper pin for speaker mode (playback only) or headset mode (playback plus recording)
- For headset mode, USB audio function topology has 2 input terminals, 2 output terminals, 1 mixer unit, 1 selector unit and 3 feature units
- Jumper pin allows for mixer unit enable/disable when in headset mode
- For speaker mode, the USB audio topology has 1 input terminal, 1 output terminal and 1 feature unit
- Supports one control endpoint, one isochrous OUT endpoint, one isochrous IN endpoint, and one interrupt IN endpoint
- Alternate zero bandwidth setting for releasing playback bandwidth on USB Bus when device is inactive
- Anti-pop noise design for device plugged and vice-versa, while A-A path is off
- Supports AES/EBU, IEC60958, S/PDIF consumer formats for stereo PCM data at S/PDIF output
- Volume up, volume down, and playback mute pins support USB HID for host control synchronization
- Record mute pin with LED indicator for record mute status
- Includes external EEPROM interface for Vendor Specific USB VID, PID, Product String, Manufacture String, and max/min/initial volumes
- 3 GPIO pins with read/write via HID interface
- Jumper pin to set the power mode (100mA or 500mA, Bus-powered or self-powered)
- Isochronous transfer uses adaptive mode with internal PLL for synchronization
- 48K/44.1KHz sampling rate for both playback and recording
- Soft mute function






- Embedded 16-bit ADC input with microphone boost
- Embedded power-on reset block
- Embedded 5V to 3.6V/3.3V/1.8V regulators for single external 5V power
- 48-pin LQFP package



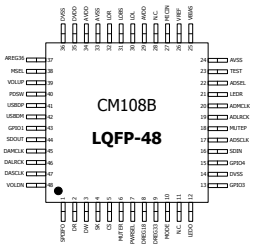



## 4 Pin descriptions

### 4.1 Pin assignment by pin number

| Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|---|---|---|---|
| 1 | SPDIFO | 13 | GPIO3 | 25 | VBIAS | 37 | AREG36 |
| 2 | DR | 14 | DVSS | 26 | VREF | 38 | MSEL |
| 3 | DW | 15 | GPIO4 | 27 | MICIN | 39 | VOLUP |
| 4 | SK | 16 | SDIN | 28 | N.C. | 40 | PDSW |
| 5 | CS | 17 | ADSCLS | 29 | AVDD | 41 | USBDP |
| 6 | MUTER | 18 | MUTEP | 30 | LOL | 42 | USBDM |
| 7 | PWRSEL | 19 | ADLRCK | 31 | LOBS | 43 | GPIO1 |
| 8 | DREG18 | 20 | ADMCLK | 32 | LOR | 44 | SDOUT |
| 9 | DREG33 | 21 | LEDR | 33 | AVSS | 45 | DAMCLK |
| 10 | MODE | 22 | ADSEL | 34 | AVDD | 46 | DALRCK |
| 11 | N.C. | 23 | TEST | 35 | DVDD | 47 | DASCLK |
| 12 | LEDO | 24 | AVSS | 36 | DVSS | 48 | VOLDN |

### 4.2 Pin-out diagram




Pin Assignments (top view)

### 4.3 Pin signal descriptions

| Pin # | Symbol | Type | Description |
|---|---|---|---|
| 1 | SPDIFO | DO, 4mA, SR | SPDIF output |
| 2 | DR | DI, 8mA, PD, 5VT | EEPROM interface data read from EEPROM |
| 3 | DW | DO, 4mA, SR | EEPROM interface data write to EEPROM |
| 4 | SK | DO, 4mA, SR | EEPROM interface clock |
| 5 | CS | DO, 4mA, SR | EEPROM interface chip select |
| 6 | MUTER | DI, ST, PU | Mute recording (edge trigger with de-bouncing) |
| 7 | PWRSEL | DI, ST, PU | Chip power select pin:<br>H: push up to 3.3V, L: push down to ground<br>Speaker mode - H: 100mA self-powered, L: 500mA Bus-powered<br>Headset mode - H: 100mA Bus-powered, L: 500mA Bus-powered |
| 8 | DREG18 | P | 1.8V Regulator Output for Digital Core |
| 9 | DREG33 | P | 3.3V Regulator Output for Digital I/O (driving current 40mA) |
| 10 | MODE | DI, ST, PD | Operating mode selection:<br>H: push up to 3.3V, L: pull down to ground<br>H: speaker mode - playback only<br>L: headset mode - playback & recording |
| 11 | N.C. | | |
| 12 | LEDO | DO, SR, 4mA | LED operation light: output H for power on, toggling for data transmit |
| 13 | GPIO3 | DIO, 8mA, PD, 5VT | GPIO pin |
| 14 | DVSS | P | Digital ground |
| 15 | GPIO4 | DIO, 8mA, PD, 5VT | GPIO pin |
| 16 | SDIN | DIO, 8mA, PD, 5VT | ADC I2S data input |
| 17 | ADSCLK | DO, 2mA, SR | ADC I2S serial clock |
| 18 | MUTEP | DI, ST, PU | Mute playback (edge trigger with de-bouncing) |
| 19 | ADLRCK | DO, 2mA, SR | ADC I2S left/right clock |
| 20 | ADMCLK | DO, 2mA, SR | 11.2896MHz output for 44.1KHz sampled data and<br>12.288MHz output for 48KHz sampled data |
| 21 | LEDR | DO, SR, 4mA | LED for mute recording indicator, output H when recording is muted |
| 22 | ADSEL | DI, ST, PD | ADC input source select pin<br>H: use external (via I2S) ADC<br>L: use internal ADC<br>(H: push up to 3.3V, L: push down to ground) |
| 23 | TEST | DI, ST, PD | Test mode select pin,<br>H: test mode<br>L: normal operation<br>(H: push up to 3.3V, L: push down to ground) |
| 24 | AVSS | P | Analog ground |
| 25 | VBIAS | AO | Microphone bias voltage supply (3V), with a small driving capability |
| 26 | VREF | AO | Connecting to external decoupling capacitor for embedded bandgap circuit, 1.75V output |
| 27 | MICIN | AI | Microphone input, input impedance is 10k Ohm |
| 28 | N.C. | | |
| 29 | AVDD | P | 5V analog power for analog circuit |
| 30 | LOL | AO | Line out: left channel |
| 31 | LOBS | AO | DC 1.75V output for line out bias |
| 32 | LOR | AO | Line out: right channel |
| 33 | AVSS | P | Analog ground |
| 34 | AVDD | P | 5V power supply for analog circuit |
| 35 | DVDD | P | 5V power supply for internal regulator |
| 36 | DVSS | P | Digital ground |
| 37 | AREG36 | P | 3.6V analog power for analog circuit |





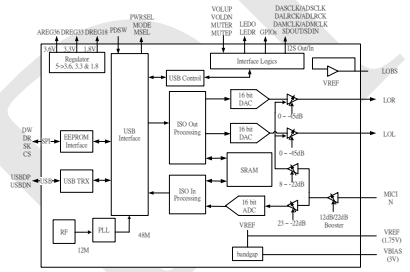

| | | | |
|---|---|---|---|
| 38 | MSEL | DI, ST, PU | Mixer enable select:<br>H: push up to 3.3V, L: push down to ground<br>H: with mixer/AA-path enabled (with default mute)<br>L: without mixer/AA-path disabled<br>USB descriptors will also be changed accordingly |
| 39 | VOLUP | DI, ST, PU | Volume up (edge trigger with de-bouncing) |
| 40 | PDSW | DO, 4mA , OD | Power down switch control signal (for PMOS polarity)<br>0: normal operation<br>1: power down mode (suspend mode) |
| 41 | USBDP | AIO | USB Data D+ |
| 42 | USBDM | AIO | USB Data D- |
| 43 | GPIO1 | DIO, 8mA, PD, 5VT | GPIO pin |
| 44 | SDOUT | DO, 2mA, SR | DAC I2S data output |
| 45 | DAMCLK | DO, 2mA, SR | 11.2896 MHz output for 44.1KHz sampled data and<br>12.288 MHz output for 48KHz sampled data |
| 46 | DALRCK | DO, 2mA, SR | DAC I2S left/right clock |
| 47 | DASCLK | DO, 2mA, SR | DAC I2S serial clock |
| 48 | VOLDN | DI, ST, PU | Volume down (edge trigger with de-bouncing) |

NoteU: DI / DO / DIO - Digital Input / Output / Bi-Directional Pad
AI / AO / AIO - Analog Input / Output / Bi-Directional Pad
SR - Slew Rate Control
ST - Schmitt Trigger
PD / PU - Pull Down / Pull Up
5VT - 5 Volt Tolerant (3.3V Pad)
OD - Open Drain
P - Power Supply Pin






## 5 Block diagram




CM108B Block Diagram

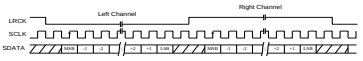





## 6 I2S Interface

The CM108B provides an I2S interface for both playback and recording. External ADC, DAC, or DSP can be added to provide additional functions within the USB audio system. The CM108B sends out master clock (fixed at x256), LRCK (fixed at x64), and data clock data. Therefore, external ADCs, DACs, or DSPs should be set to slave mode.

The left channel of the CM108B's I2S bus is used for mono recording. Both IP$^{2P}$S buses use a 5V tolerant pad in order to easily interface with 5V or 3.3V devices. Playback data is simultaneously sent to both the DAC and I2S bus. The recording source (ADC or I2S bus) can be selected by ADSEL jumper pin.



# J. CM119 Datasheet



## 1.DESCRIPTIONS AND OVERVIEW

CM119 is a highly integrated single chip USB audio controller specifically for VoIP (Voice over internet protocol) application. All essential analog modules are embedded in CM119, including dual DAC and earphone driver, ADC, microphone booster, PLL, regulator, and USB transceiver. 8 GPIO pins can constitute a 24 key matrix directly support keypad control function without MCU. It's also support buzzer output pin for VoIP application. In addition, audio adjustment can be easily controlled via specific HID compliant volume control pins. Many features are programmable with jumper pins or external EEPROM. Vender can customized unique USB VID/PID to EEPROM for VoIP software authentication. Moreover, individual unique phone number for each device is possible via serial number stored in external EEPROM. Moreover, CM119 provided I2C interface with MCU application for LCM integrated and advanced functions.

VoIP applications are becoming increasing popular as VoIP can provide free or low-cost calling worldwide. To provide a VoIP experience that is the same as using a regular phone and eliminate the poor call quality that results from using the PC audio, C-Media has developed CM119 USB Controller that enables a regular phone, handset, or headset which is interfaced to the USB port on the PC. With the C-Media OEMs can quickly bring to market a family of low cost high quality VoIP products.

## 2. FEATURES

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB Audio Device class specification v1.0
- Supports USB Suspend/Resume Mode and remote Wakeup with Volume Control pins
- Single 12MHz Crystal input with on-chip PLL and embedded USB transceiver
- Jumper Pin for Speaker Mode (Playback Only) or Headset Mode (Playback + Recording)
- For Headset Mode, USB audio function topology has 2 Input Terminals, 2 Output Terminals, 1 Mixer Unit, 1 Selector Unit, and 3 Feature Units
- Jumper Pin for Operation System Mixer Unit Enable/Disable under Headset Mode







- For Speaker Mode, USB audio function topology has 1 Input Terminal, 1 Output Terminal, and 1 Feature Unit
- Support one Control Endpoint, one Isochroous out Endpoint, one Isochroous in Endpoint, and one Interrupt in Endpoint
- Alternate zero bandwidth setting for releasing playback bandwidth on USB Bus when this device is inactive
- Volume up, volume down, and playback mute support USB HID for Host Control Synchronization
- Record Mute Pin with LED Indicator for Record Mute Status
- External EEPROM Interface for Vendor Specific USB VID, PID, and Serial Number
- Supports AES/EBU, IEC60958, S/PDIF Consumer Formats for Stereo PCM Data at S/PDIF Output
- 8 GPIO Pins with Read/Write via HID
- Embedded Buzzer Function controlled by Register
- Support I2C Interface for External MCU Integrated
- Jumper Pin for Output Voltage Swing (3.5V or 2.5V)
- Jumper Pin for Power Mode Setting
- Isochroous transfer uses Adaptive Mode with Internal PLL for Synchronization
- 48K/44.1KHz Sampling Rate for both Playback and Recording
- Soft Mute Function
- Embedded High Performance 16 bit audio DAC with Earphone Phone Buffer
- Host side data loss noise reduction function
- Embedded 16 bit ADC input with Microphone Boost
- Embedded power on Reset Block
- Embedded 5V to 3.3V regulator for single External 5V Operation
- Compatible with Win98 SE / Win ME / Win 2000 / Win XP and Mac OS9 / OS X without Additional Driver
- 48 Pin LQFP Package
- Support Hardware SDK tool for third-party software or soft-phone development





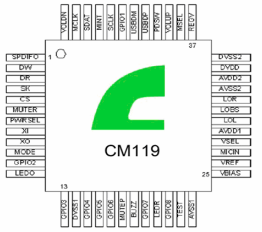


## 3. PIN DESCRIPTIONS

### 3.1 PIN ASSIGNMENT BY PIN NUMBER

| Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|---|---|---|---|
| 1 | SPDIFO | 13 | GPIO3 | 25 | VBIAS | 37 | REGV |
| 2 | DW | 14 | DVSS1 | 26 | VREF | 38 | MSEL |
| 3 | DR | 15 | GPIO4 | 27 | MICIN | 39 | VOLUP |
| 4 | SK | 16 | GPIO5 | 28 | VSEL | 40 | PDSW |
| 5 | CS | 17 | GPIO6 | 29 | AVDD1 | 41 | USBDP |
| 6 | MUTER | 18 | MUTEP | 30 | LOL | 42 | USBDM |
| 7 | PWRSEL | 19 | BUZZ | 31 | LOBS | 43 | GPIO1 |
| 8 | XI | 20 | GPIO7 | 32 | LOR | 44 | SCLK |
| 9 | XO | 21 | LEDR | 33 | AVSS2 | 45 | MINT |
| 10 | MODE | 22 | GPIO8 | 34 | AVDD2 | 46 | SDAT |
| 11 | GPIO2 | 23 | TEST | 35 | DVDD | 47 | MCLK |
| 12 | LEDO | 24 | AVSS1 | 36 | DVSS2 | 48 | VOLDN |

### 3.2 PIN-OUT DIAGRAM




Pin Assignments (Top View)







### 3.3 PIN SIGNAL DESCRIPTIONS

| Pin # | Symbol | Type | Description |
|---|---|---|---|
| 1 | SPDIFO | DO, 8mA, SR | SPDIF Output |
| 2 | DW | DIO, 8mA, PD, 5VT | USB Controller Data Read From EEPROM Interface.<br>EEPROM Data Output. |
| 3 | DR | DO, 4mA, SR | USB Controller Data Writes to EEPROM Interface.<br>EEPROM Data Input. |
| 4 | SK | DO, 4mA, SR | EEPROM Interface Clock (100KHz) |
| 5 | CS | DO, 4mA, SR | EEPROM Interface Chip Select |
| 6 | MUTER | DI, ST, PU | Mute Recording (Edge Trigger with de-Bouncing) |
| 7 | PWRSEL | DI, ST | H: Pull Up to 3.3V; L: Pull Down to Ground<br>Speaker Mode H：Self Power with 100mA：L：Bus Power with 500mA<br>Headset Mode H：Bus Power with 100mA：L：Bus Power with 500mA |
| 8 | XI | DI | Input Pin for 12MHz Oscillator |
| 9 | XO | DO | Output Pin for 12MHz Oscillator |
| 10 | MODE | DI, ST | H: Pull Up to 3.3V; L: Pull Down to Ground<br>L：Headset Mode: Playback & Recording<br>H：Speaker Mode: Playback Only |
| 11 | GPIO2 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 12 | LEDO | DO, SR, 8mA | LED for Operation; Output H for Power On; Toggling for Data Transmit |
| 13 | GPIO3 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 14 | DVSS1 | P | Digital Grounding |
| 15 | GPIO4 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 16 | GPIO5 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 17 | GPIO6 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 18 | MUTEP | DI, ST, PU | Mute Playback (Edge Trigger with de-Bouncing) |
| 19 | BUZZ | DO, 8mA, SR | Buzzer Output Pin |
| 20 | GPIO7 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 21 | LEDR | DO, SR, 8mA | LED for Mute Recording Indicator; Output H when Recording is Muted |
| 22 | GPIO8 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 23 | TEST | DI, ST, PD | Test Mode Select Pin; Pull Low for Normal Operation |
| 24 | AVSS1 | P | Analog Ground |

| | | | |
|---|---|---|---|
| 25 | VBIAS | AO | Microphone Bias Voltage Supply (4.5V) |
| 26 | VREF | AO | Connecting to External Decoupling Capacitor for Embedded Bandgap Circuit; 2.25V Output |
| 27 | MICIN | AI | Microphone Input |
| 28 | VSEL | AI | Line Out Voltage Swing Select<br>H: Pull Up to 5V, L: Pull Down to Ground<br>L: 2.5Vpp Output；H: 3.5Vpp Output |
| 29 | AVDD1 | P | 5V Analog Power for Analog Circuit |
| 30 | LOL | AO | Line Out Left Channel |
| 31 | LOBS | AO | DC 2.25V Output for Line Out Bias |
| 32 | LOR | AO | Line Out Right Channel |
| 33 | AVSS2 | P | Analog Ground |
| 34 | AVDD2 | P | 5V Analog Power for Analog Circuit |
| 35 | DVDD | P | 5V Power Supply to Internal Regulator |
| 36 | DVSS2 | P | Digital Grounding |
| 37 | REGV | AO | 3.3V Reference Output for Internal 5V → 3.3V Regulator |
| 38 | MSEL | DI, ST | Mixer Enable Select<br>H: Pull Up to 3.3V, L: Pull Down to Ground<br>L: Without Mixer; H: With Mixer (With Default Mute)<br>USB Descriptors are changed accordingly |
| 39 | VOLUP | DI, ST, PU | Volume Up (Edge Trigger with de-Bouncing) |
| 40 | PDSW | DO, 4mA , OD | Power Down Switch Control (for PMOS Polarity)<br>0: Normal Mode, 1: Power Down Mode |
| 41 | USBDP | AIO | USB Data D+ |
| 42 | USBDM | AIO | USB Data D- |
| 43 | GPIO1 | DIO, 8mA, PD, 5VT | GPIO Pin |
| 44 | SCLK | DIO, 8mA, PD, 5VT | External MCU Serial Bus Clock Pin |
| 45 | MINT | DO, 4mA, SR | External MCU Interrupt Pin<br>When Register Address 4 ~ 7 has new data, MINT is set Low; after MCU read MINT is reset to H |
| 46 | SDAT | DIO, 8mA, PD, 5VT | External MCU Serial Bus Data Pin |
| 47 | MCLK | DO, 4mA, SR | External MCU Clock Pin, Clock Frequency is Programmable<br>Default is 1.5 MHz (Options Include, 6MHz, 3MHz, 1.5MHz) |
| 48 | VOLDN | DI, ST, PU | Volume Down (Edge Trigger with de-Bouncing) |





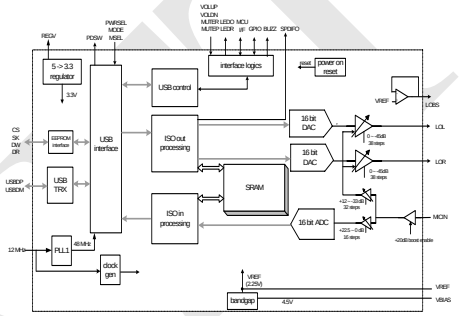


**Note:** DI – Digital Input Pad, DO – Digital Output Pad, DIO – Digital bi-Directional Pad, AI/AO/AIO – Analog Pad, SR Slew Rate Control, ST – Schmitt Trigger, PD/PU – Pull Down or Pull Up, 5VT – 5 Volt Tolerant (3.3V Pad), OD – Open Drain

## 4. MCU INTERFACE

CM119 provides a serial MCU Interface for external MCU to access internal registers with these registers access. MCU and host side software can have bi-directional communication. This interface can keep flexibility for external module control and integrate, such as LCD panel.

## 5. BLOCK DIAGRAM




**Block Diagram Of CM119**







## 7. FUNCTION DESCRIPTIONS

### 7.1 USB Interface

CM119 integrates USB transceiver, PLL, and regulator so only a few passive components are necessary for the USB interface connection. Default USB descriptors are embedded in CM119; therefore no additional design effort is needed for a generic USB operation. PID changes with the jumper pin setting so different setting have different PID. For customized product, customer can attach a 93C46 EEPROM to override the embedded VID, PID and provide addition serial number for each set. CM119 automatically detects 93C46 existence and performs the overwrite function during power up.

#### 7.1.1 Device Descriptor

| Offset | Field | Size | Value (Hex) | Description |
|---|---|---|---|---|
| 0 | bLength | 1 | 12 | Total 18 Bytes |
| 1 | bDescriptorType | 1 | 01 | Device Descriptor |
| 2 | bcdUSB | 2 | 0110 | USB 1.1 compliant. |
| 4 | bDeviceClass | 1 | 00 | |
| 5 | bDeviceSubClass | 1 | 00 | |
| 6 | bDeviceProtocol | 1 | 00 | |
| 7 | bMaxPacketSize0 | 1 | 40 | Endpoint zero Size = 64 bytes |
| 8 | idVendor | 2 | 0d8c | Vendor ID |
| 10 | idProduct | 2 | 0008 – 000F | Product ID<br>Programmable by MSEL and MODE pin |
| 12 | bcdDevice | 2 | 0100 | Device compliant to the Audio Device Class specification version 1.00 |
| 14 | iManufacturer | 1 | 01 | Index of string descriptor describing manufacturer |
| 15 | iProduct | 1 | 02 | Index of string descriptor describing product |
| 16 | iSerialNumber | 1 | 03 | Index of string descriptor describing the device's serial number |
| 17 | bNumConfigurations | 1 | 01 | Configurations number = 1 |

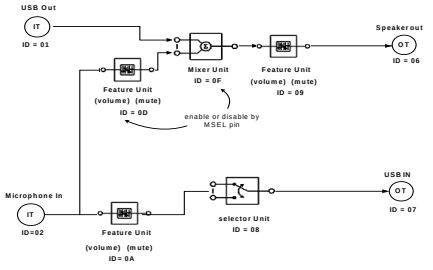
**Note**: VID, PID, and serial number can be overridden by external EEPROM content







#### 7.1.4 USB Audio Topology Diagram




**USB Audio Topology Diagram**

### 7.2 Jumper Pins and Mode Setting:

Several jumper pins can set the configuration of CM119. These jumper pin settings affect both USB descriptors and USB audio topology. If MODE pin is pulled up to 3.3V (speaker mode), a playback only function is activated and there is no recording function declared to the host. At this setting, MSEL pin is ignored and only one input terminal, one output terminal and one feature unit is declared in USB audio topology.

If MODE pin is pulled low (headset mode), a full duplex playback and recording function is reported to the host. MSEL pin setting activates one mixer unit and one feature unit. The following USB audio topology in Chapter: 7.1.4 is an example of headset mode. PWRSEL pin affects the power configuration of CM119; together with MODE pin totally 4 combinations are programmable.

# K. CH340 Datasheet

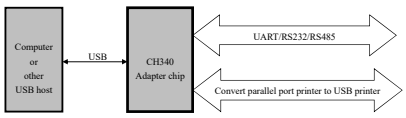


**USB to Serial Port chip CH340**

Datasheet
Version: 3C
https://wch-ic.com

## 1. Overview

CH340 is a USB bus adapter chip, can realize USB to serial port or USB to print port.
In serial port mode, CH340 provides commonly used MODEM contact signals, which are used to expand asynchronous serial ports for computers, or directly upgrade ordinary serial port devices to the USB bus. For instructions on USB to print port, please refer to manual (2) CH340DS2.



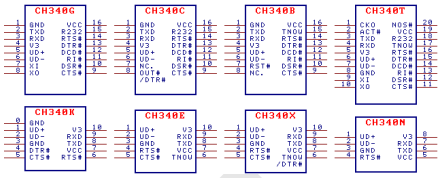

## 2. Features

- Full-speed USB device interface, compatible with USB V2.0.
- Simulation of standard serial ports, used to upgrade original serial port peripherals, or add additional serial ports through USB.
- The serial port application program under the Windows operating system on the computer side is fully compatible, no need to be modified.
- Hardware full-duplex serial port, built-in transceiver buffer, supports communication baud rate of 50bps~2Mbps.
- Support commonly used MODEM contact signals RTS, DTR, DCD, RI, DSR, CTS
- Provide RS232, RS485, RS422 interfaces by adding level conversion devices.
- CH340R supports IrDA specification SIR infrared communication, and baud rate from 2400bps to 115200bps.
- Built-in firmware, and software compatible with CH341, you can use the VCP driver of CH341 directly.
- Support 5V and 3.3V supply voltage.
- CH340C/N/K/E/X/B has a built-in clock, requires no external crystal. CH340B also has a built-in EEPROM for configuring the serial number.
- SOP-16, SOP-8 and SSOP-20, ESSOP-10, MSOP-10 lead-free packages are available, RoHS compatible.





## 3. Package




| Package | Shaping Width | | Pin Spacing | | Package Description | Order Model |
|---|---|---|---|---|---|---|
| SOP-16 | 3.9mm | 150mil | 1.27mm | 50mil | Small Out-Line Package | CH340G |
| SOP-16 | 3.9mm | 150mil | 1.27mm | 50mil | Small Out-Line Package | CH340C |
| SOP-16 | 3.9mm | 150mil | 1.27mm | 50mil | Small Out-Line Package | CH340B |
| SOP-8 | 3.9mm | 150mil | 1.27mm | 50mil | Small Out-Line Package | CH340N |
| ESSOP-10 | 3.9mm | 150mil | 1.00mm | 39mil | Exposed Shrink Small Outline Package | CH340K |
| MSOP-10 | 3.0mm | 118mil | 0.50mm | 19.7mil | Miniature Small Outline Package | CH340E |
| MSOP-10 | 3.0mm | 118mil | 0.50mm | 19.7mil | Miniature Small Outline Package | CH340X |
| SSOP-20 | 5.3mm | 209mil | 0.65mm | 25mil | Shrink Small Outline Package | CH340T |
| SSOP-20 | 5.3mm | 209mil | 0.65mm | 25mil | Shrink Small Outline Package | CH340R |

*Note: CH340C, CH340N, CH340K, CH340E, CH340X and CH340B have a built-in clock and do not require an external crystal.*

*CH340B has a built-in EEPROM for configuration of the serial number, as well as some of the functions can be customized, etc. The CH343P is recommended for smaller sizes.*

*CH340K has three built-in diodes to prevent the MCU from backing up current to the CH340 through the I/O pins when it is powered independently.*

*CH340K's backplane is pin 0#GND, an optional connection; pin 3#GND is a required connection.*

*CH340X is improved based on the CH340E by adding the IO tolerant 5V feature for 3.3V supply.*

*CH340X pin 6# can be switched from TNOW to DTR# if an external resistor is added; see Section 5.3 for details of the two configurations.*

*CH340C can be switched from TNOW to DTR# by adding a 4.7KΩ pull-down resistor to pin 8# if the lot number starts with 4 and the last 3 bits are greater than B40.*

*CH340R provides reverse polarity TXD and MODEM signals and has been discontinued.*

*CH340's USB transceiver is designed to be fully internalized according to USB2.0, and it is recommended that the UD+ and UD- pins are not connected with additional resistors.*





## 4. Pin

| SSOP20 Pin No. | SOP16 Pin No. | ESSOP10 Pin No. | SOP8 Pin No. | Pin name | Type | Pin description (The description in brackets is only for the CH340R model) |
|---|---|---|---|---|---|---|
| 19 | 16 | 7 | 5 | VCC | Power | Positive power input terminal, requires an external 0.1uF power decoupling capacitor. |
| 8 | 1 | 3、0 | 3 | GND | Power | Common ground, directly connected to the ground of the USB bus |
| 5 | 4 | 10 | 8 | V3 | Power | When the power supply voltage is 3.3V, connect VCC to input the external power supply. When the power supply voltage is 5V, connect an external decoupling capacitor with a capacity of 0.1uF. |
| 9 | 7 | None | None | XI | Input | CH340T/R/G: The input terminal of crystal oscillation requires an external 12MHz crystal and oscillation capacitor. |
| | | | | NC. | Empty pin | CH340C: Empty pin, must be suspended |
| | | | | RST# | Input | CH340B: External reset input, active low, built-in pull-up resistor |
| 10 | 8 | None | None | XO | Output | CH340T/R/G: The output terminal of crystal oscillation needs to be connected to an external 12MHz crystal and oscillation capacitor. |
| | | | | OUT# | Output | CH340C: MODEM general output signal, software defined, active low. Some lot of CH340C can optionally be switched to the second DTR# |
| | | | | NC. | Empty pin | CH340B: Empty pin, must be suspended |
| 6 | 5 | 1 | 1 | UD+ | USB signal | Connect directly to the D+ data line of the USB bus without a series resistor |
| 7 | 6 | 2 | 2 | UD- | USB signal | Connect directly to the D- data line of the USB bus without a series resistor |
| 20 | None | None | None | NOS# | Input | Disable USB device suspension, active low, built-in pull-up resistor |
| 3 | 2 | 8 | 6 | TXD | Output | Serial data output (CH340R model is inverted output) |
| 4 | 3 | 9 | 7 | RXD | Input | Serial data input with built-in controllable pull-up and pull-down resistors |
| 11 | 9 | 5 | None | CTS# | Input | MODEM contact input signal, clear to send, active low (high) |
| 12 | 10 | None | None | DSR# | Input | MODEM contact input signal, data device ready, active low (high) |
| 13 | 11 | None | None | RI# | Input | MODEM contact input signal, ringing indication, active low (high) |
| 14 | 12 | None | None | DCD# | Input | MODEM contact input signal, carrier detection, |





| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | active low (high) |
| 15 | 13 | 4 | None | DTR# | Output | MODEM contact output signal, data terminal ready, active low (high) |
| 16 | 14 | 6 | 4 | RTS# | Output | MODEM contact output signal, request to send, active low (high) |
| 2 | None | None | None | ACT# | Output | USB configuration completion status output, active low |
| 18 | 15 | None | None | R232 | Input | CH340T/R/G/C: Auxiliary RS232 enable, active high level, built-in pull-down |
| 17 | 15 | None | None | TNOW | Output | CH340T/E/X/B: The serial port sends ongoing status indication, high level is active. CH340X external resistor can be switched to DTR# |
| | | | | IR# | Input | CH340R: Serial port mode setting input, built-in pull-up resistor, low level is SIR infrared serial port, high level is ordinary serial port |
| 1 | None | None | None | CKO | Output | CH340T: clock output |
| | | | | NC. | Empty pin | CH340R: Empty pin, must be suspended |

*Note: The unused I/O pins of CH340 can be dangled. The application diagram is an example of CH340T, etc., and also applies to CH340G/C/N/K/E/X/B, etc.*

## 5. Function Description

### 5.1 Clock, Reset, Power, Connection

When the CH340G/CH340T/CH340R chip works normally, it requires an external 12MHz clock signal to be provided to the XI pin. Under normal circumstances, the clock signal is generated by the built-in inverter of CH340 through stable frequency oscillation of the crystal. The peripheral circuit only needs to connect a 12MHz crystal between the XI and XO pins, and connect the oscillation capacitors from the XI and XO pins to ground respectively.
CH340C/N/K/E/X/B chips have built-in clock generators, no need for external crystals and capacitors.
The CH340 chip has a built-in power-on reset circuit. The CH340B chip also provides an active low-level external reset input pin.
The CH340 chip supports 5V power supply voltage or 3.3V power supply voltage. When using a 5V operating voltage, the VCC pin of the CH340 chip inputs an external 5V power supply, and the V3 pin should be connected to an external power supply decoupling capacitor with a capacity of 0.1uF. When using a 3.3V working voltage, the V3 pin of the CH340 chip should be connected to the VCC pin, and an external 3.3V power supply should be input at the same time, and the working voltage of other circuits connected to the CH340 chip should not exceed 3.3V.
The IO of CH340X and CH340C/N starting with lot number 4 support 5V withstand voltage to prevent inward current flow.
CH340K not only prevents inward current backflow, but also reduces the external drive capability, which can reduce the outward current backflow of CH340.
The CH340 chip automatically supports USB device suspension to save power consumption. When the NOS# pin is low level, USB device suspension will be prohibited.
The DTR# pin of the CH340G/C/T/K chip is used as a configuration input pin before the USB configuration is completed. It can be connected to an external 4.7KΩ pull-down resistor to generate a default low level during USB enumeration and send it to the USB bus through the configuration descriptor. Apply for larger supply current.
The CH340 chip has a built-in USB pull-up resistor, and the UD+ and UD- pins should be directly connected to the USB bus.
The pins of the CH340 chip in asynchronous serial port mode include: data transmission pins, MODEM contact signal pins, and auxiliary pins.
Data transmission pins include: TXD pin and RXD pin. When the serial port input is idle, RXD should be high level.
For the CH340G/C/T/R chip, if the R232 pin is high level to enable the auxiliary RS232 function, then an inverter is automatically inserted inside the RXD pin, which defaults to low level. When the serial port output is idle, the TXD of the CH340G/C/N/E/X/B/T chip is high level, the TXD of the CH340K chip is a weak high level, and the TXD of the CH340R chip is low level.
MODEM contact signal pins include: CTS# pin, DSR# pin, RI# pin, DCD# pin, DTR# pin, RTS# pin, CH340C also provides OUT# pin. All these MODEM contact signals are controlled and defined by computer applications.
Auxiliary pins include: IR# pin, R232 pin, CKO pin, ACT# pin, TNOW pin. A low level on the IR# pin will enable the infrared serial port mode. The R232 pin is used to control the auxiliary RS232 function. When R232 is high level, the RXD pin input is automatically inverted. The ACT# pin is the USB device configuration completion status output (such as USB infrared adapter ready). The TNOW pin indicates that the CH340 is sending data from the serial port with a high level, and becomes low level after the transmission is completed. In half-duplex serial port modes such as RS485, TNOW can be used to indicate the serial port transceiver switching status. The IR# and R232 pins are only checked once after power-on reset.

### 5.2 CH340B Configuration Information

The CH340B chip also provides an EEPROM configuration data area. Product serial number and other information





can be set for each chip through special computer tool software. The configuration data area is shown in the table below.

| Byte address | Abbreviation | Description of the configuration data area | Default value |
|---|---|---|---|
| 00H | SIG | For CH340B: The internal configuration information valid flag must be 5BH.<br>For CH340H/S: The external configuration chip valid flag must be 53H. Other values are invalid. | 00H |
| 01H | MODE | Serial port mode, must be 23H | 23H |
| 02H | CFG | Specific configuration, bit 5 is used to configure the product serial number string: 0=valid; 1=invalid | FEH |
| 03H | WP | Internal configuration information write protection flag, if it is 57H, it is read-only, otherwise it can be rewritten. | 00H |
| 05H–04H | VID | Vendor ID, vendor identifier, high byte follows, any value. Set to 0000H or 0FFFFH to use vendor defaults for VID and PID. | 1A86H |
| 07H–06H | PID | Product ID, product identification code, high byte last, any value | 7523H |
| 0AH | PWR | Max Power, maximum supply current in 2mA increments | 31H |
| 17H–10H | SN | Serial Number, product serial number ASCII string, length 8. Serial number is disabled if the first byte is not an ASCII character (21H to 7FH). | 12345678 |
| 3FH–1AH | PROD | For CH340B: Product String, product description Unicode string. The first byte is the total number of bytes (not exceeding 26H), the second byte is 03H, and the following is a Unicode string. If it does not meet the above characteristics, the manufacturer's default instructions will be used. | The first byte 00H uses the default product description |
| Other addresses | | (Reserved unit) | 00H or FFH |

### 5.3 DTR and Multi-Mode MCUs Download

For CH340X, pin 6# defaults to TNOW, which has a weak pull-up during power-on or reset. During normal operation, the TNOW output is used for half-duplex transceiver switching. By adding an external resistor to the 6# pin, TNOW can be switched to DTR#. The two options are as follows:

① If the 6# pin is connected to an external 4.7K Ω pull-down resistor to GND, it will enter the open source DTR enhancement mode, and the 6# pin will automatically switch to the open source driven DTR# for connecting to the BOOT mode pin of the MCU. The default DTR# is It is not output and is kept low by an external resistor, but the DTR# pin can be set by the application program to output a high level or not. It is used for multi-mode MCU downloads where DTR# defaults to a low level.

② If a 4.7KΩ resistor is connected between the 6# pin and the 5# pin, it will enter the push-pull DTR enhancement mode, and the 6# pin will automatically switch to the push-pull driven DTR# for connecting to the control pin of the MCU. The DTR# pin can be set to output high level or low level by the application program, which is used for multi-mode MCU download with DTR# default high level.

For CH340C whose lot number starts with 4 and whose last three digits are greater than B40, pin 8# defaults to OUT#, has a weak pull-up during power-on or reset, and is the OUT# output of MODEM during normal operation. If an external 4.7KΩ pull-down resistor is connected to the 8# pin, it will enter the open source DTR enhancement





mode. The 8# pin will automatically switch to the second DTR# of the open-source driver for connecting to the BOOT mode of the MCU. The default second DTR# is not output, is kept low by an external resistor, but this DTR# pin can be set by the application to output high level or not, for multi-mode MCU downloads where DTR# defaults to low level. In addition, the original DTR# of pin 13# is used for multi-mode MCU download with DTR# default high level.

### 5.4 Serial Port Characteristics

CH340 has a built-in independent transceiver buffer and supports simplex, half-duplex or full-duplex asynchronous serial communication. Serial data includes 1 low-level start bit, 5, 6, 7 or 8 data bits, 1 or 2 high-level stop bits, and supports odd/even/flag/blank check test. CH340 supports common communication baud rates: 50, 75, 100, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1500000, 2000000.
For applications with one-way 1Mbps and above, or two-way 500Kbps and above, it is recommended to use CH343 to enable hardware automatic flow control.
The allowable baud rate error of the CH340 serial port receive signal is about 2%, the baud rate error of the CH340G/CH340T/CH340R serial port transmit signal is less than 0.3%, and the baud rate error of the CH340C/340N/340K/340E/340X/340B serial port transmit signal is less than 1.2%.
Under the Windows operating system on the computer side, the CH340 driver can emulate the standard serial port, so most of the original serial port applications are fully compatible and usually do not require any modification.
CH340 can be used to upgrade original serial port peripherals, or add additional serial ports to the computer through the USB bus. By adding an external level conversion device, RS232, RS485, RS422 and other interfaces can be further provided.
CH340R only needs to add an infrared transceiver, and can add a SIR infrared adapter to the computer through the USB bus to achieve infrared communication between the computer and external devices that comply with the IrDA specification.





## 6. Parameters

**6.1 Absolute Maximum Value** (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

| Name | Parameter Description | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| TA | Ambient temperature during operation | CH340G/CH340T/CH340R | -40 | 85 | ℃ |
| | | CH340C/CH340N/CH340K/CH340E/CH340B | -20 | 70 | ℃ |
| | | CH340X/Lot 4 beginning CH340C/N | -40 | 85 | ℃ |
| TS | Ambient temperature during storage | | -55 | 125 | ℃ |
| VCC | Power supply voltage (VCC is connected to the power supply, GND is connected to the ground) | | -0.5 | 6.0 | V |
| VIO | The voltage on the input or output pin | | -0.5 | VCC+0.5 | V |

**6.2 5V Electrical Parameters** (Test conditions: TA=25℃, VCC=5V, does not include pins to connect to USB bus)

| Name | Parameter Description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VCC | Power voltage | The V3 pin is only connected to an external capacitor and is not connected to VCC. | 4.0 | 5 | 5.3 | V |
| ICC | Total power supply current during operation | CH340G/C/N/K/E/X/T/R | | 7 | 20 | mA |
| | | CH340B | | 6 | 15 | mA |
| ISLP | Total supply current in USB suspended | CH340G/K/T/R/B | | 0.09 | 0.2 | mA |
| | | CH340C/N/E/X | | 0.05 | 0.15 | mA |
| VIL | low level input voltage | | 0 | | 0.9 | V |
| VIH | High level input voltage | | 2.3 | | VCC | V |
| VOL | Low level output voltage (6mA sink current) | | | | 0.5 | V |
| VOH | High-level output voltage (2mA output current)<br>(Only 100uA output current during chip reset) | | VCC-0.6 | | | V |
| IUP | Input current of input terminal with built-in pull-up resistor | | 3 | 150 | 300 | uA |
| IDN | Input current of the input terminal with built-in pull-down resistor | | -40 | -100 | -300 | uA |
| VR | Voltage threshold for power-on reset | | 2.4 | 2.6 | 2.8 | V |

**6.3 3.3V Electrical Parameters** (Test conditions: TA=25℃, VCC=V3=3.3V, does not include pins to connect

# L. Corechips SL2-1A Datasheet

**USB2.0 HUB 控制器集成电路**

**USB 2.0 HIGH SPEED 4-PORT HUB CONTROLLER**

## SL2.1A

**数据手册**

Data Sheet

深圳市和芯润德科技有限公司 V1.0

CoreChips ShenZhen CO.,Ltd

### 第一章 管脚分配

**SL2. 1A 管脚图**

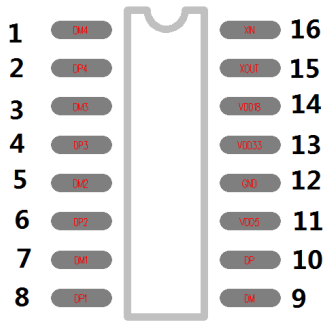



图 1：SL2.1A 管脚图

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CoreChips ShenZhen CO.,Ltd

**SL2.1A 管脚定义**

| 管脚名称 | 16 Pin# | Die | IO类型 | 定义 |
|---|---|---|---|---|
| DM4 | 1 | | B | 下行口 4 的USB DM信 号 |
| DP4 | 2 | | B | 下行口 4 的USB DP信号 |
| DM3 | 3 | | B | 下行口 3 的USB DM信号 |
| DP3 | 4 | | B | 下行口 3 的USB DP信号 |
| DM2 | 5 | | B | 下行口 2 的USB DM信号 |
| DP2 | 6 | | B | 下行口 2 的USB DP信号 |
| DM1 | 7 | | B | 下行口 1 的USB DM信号 |
| DP1 | 8 | | B | 下行口 1 的USB DP信号 |
| DM | 9 | | B | 上行口的USB DM信 号 |
| DP | 10 | | B | 上行口的USB DP信号 |
| VDD5 | 11 | | P | 5v输入 |
| GND | 12 | | P | 芯片地 |
| VDD33 | 13 | | P | 内部 3.3v |
| VDD18 | 14 | | P | 内部 1.8v |
| XOUT | 15 | | O | 晶振PAD |
| XIN | 16 | | I | |

注释： O，输出；I 输入；B 双向；P 电源/接地；

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