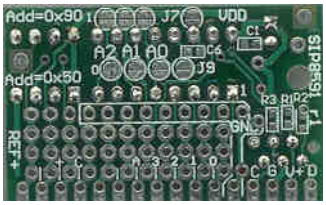
8 Bit, 4 Channel ADC, 1 DAC, 6 Digit Counter

January 16, 2013

Introduction

SIP8591 is an 8 bit ADC/DAC and 6 Digit Event Counter module based on the NXP PCF8591 ADC/DAC and PCF8593 counter.

This module does not require any surface mounted components, and the chips are very simple to understand.

Top View	Bottom View
	

The PCF8591 is probably the simplest 8 bit ADC/DAC.

- 0-VDD range
- 4 ADC channels, with single ended or differential inputs.
- 1 DAC channel
- 6 Digit Event Counter
- DIP packages for easy field replacement
- VDD is reference

The PCF8593 is an RTC[1] chip. It has an event counter mode which counts 6 BCD digits. The module does not contain any oscillator components, the PCF8593 is for use as an event counter only, not as a clock.

Contents

[1] Realtime Clock

1 PCF8591 ADC/DAC

PCF8591 Datasheet

The PCF8591 is a 4 channel 8 bit ADC, with and 8 bit 1 channel DAC output.

1.1 Reference Voltage

It does not have an internal voltage reference, and by default the module uses VDD and GND as the reference voltages. By cutting links J7 and J9 you can use external reference voltages for VRef+ and VRef-

1.2 ADC Reading Commands

The ADC inputs are read directly during the I2C read cycle. You do not have to trigger the ADC read, or wait for the results.

The base address of PCF8591 is 0x90. 8 sub-addresses are available.

Read all 4 ADC channels as single ended inputs. This sets up the control register and reads the data as a single block:

```
S90 44 R04P
```

Note that the analog output shpould be enabled, when reading multiple channels, to avod conversion errors.

To read all 4 single ended ADC values, followed by the 6 digit counter

1.3 DAC Output

To use the DAC output the output must be enabled, then the data written. The DAC output is a ratio of the reference levels, and itmay be used as a multiplier of the input level. The DAC output is mostly a low impedance <50 ohms, but rises to 400 ohms in the last few counts at each supply rail.

To write the DAC value to 0x80 end:

```
S 90 44 80 P
```

To write the DAC value to 0x80 while reading all ADC channels

```
S90 44 80 R04 P
```

DAC values can be written in a long series, one value after another. Eg a rising voltage staircase

```
S90 44 00 10 20 30 40 50 60 70 80 90 A0 B0 C0 D0 E0 F0 FF P
```

2 Prototyping Area: Dividers and Filters

There is small prototyping area. You can use this for input dividers or RC or LC filters. The pads closest to IC1 are ground pads.

Coupling capacitor or pullup/down resistors on the PCF8593 Clock In are fitted here also.

Optional Zener

You can fit Z1 the optional 6.2V protection zener where there is a chance of reversed or over voltage supply to the I2C bus, or where destructive voltages might get applied to the ADC inputs. In some cases it will prevent or limit damage spreading through the system.

3 External ADC / DAC Reference

Normally Ref+ and Ref- are VDD and GND. However J7 and J8 can be cut to use the external reference inputs. If using external reference you can fit C6 to reduce noise.

4 PCF8593 6 Digit Event Counter

PCF8593 Datasheet

The PCF8593 is a normally used as a real time clock chip. It has a 6 digit event counter mode which directly counts the input. The result is in plain BCD format. So when it is read with an I2C2PC adaptor, the numbers will be plain decimal.

4.1 Event Counter Commands

The base address of PCF8593 is 0xA2. No subaddresses are available.

To clear the counter registers and set up event counter mode send:

```
SA2 00 A0 00 00 00 00 00 00 00 00 P W 00 20 P
```

It is best to read the data back directly as a 6 digit decimal number, with the digits in the correct sequence (MSD .. LSD):

```
SA2 03 R01 W02 R01 W01 R01 P
```

If you want the simplest command to read the event counter, however data is returned as D1 D0 D3 D2 D5 D4 :

```
SA2 01 R 06 P
```

4.2 Alarm and Timer Registers

You can use the alarm compare registers to setup a hardware alert when a count is reached.
The timer registers can be used to create periodic output at some division rate.

4.3 Clock Input Circuit

The clock input of the PCF8593 is an oscillator stage with feedback. It should not be left floating. You can use it in these ways:

- Drive direct with logic input
- Pull up resistor to VDD, external switch or opto to gnd
- Pull down resistor to gnd, external switch or opto to VDD
- capacitor coupled

Maximum input frequency is 1MHz. Input capcitance is 25pF.

To check that the input is being conditioned correctly you can put an oscilloscope on pin2, Clock Out.

4.4 Extended Counting

Event counting mode allows a maximum count of 1 million.

The 50Hz clock mode will give a direct count of all edges. This gives a maximum count of 6.3e9, or 9 effective digits. The data will be in clock format (h:m:s,d:m:y), so a conversion to decimal will be required. However if a very large count is required this is an option.

You may also use the 32.768kHz clock mode, which provides an effective prescale of 327.68

5 I2C Communications

The base address of PCF8591 is 0x90. 8 sub-addresses are available through J1-6.

Address	J1 (A0 H)	J2 (A1 H)	J3 (A2 H)	J4 (A0 L)	J5 (A1 L)	J6 (A2 L)
0x90				X	X	X
0x92	X				X	X
0x94		X		X		X
0x96	X	X				X
0x98			X	X	X	
0x9A	X		X		X	
0x9C		X	X	X		
0x9E	X	X	X			

The address of PCF8593 is 0xA2. There are no other subaddresses available. If you need more counters use our Bus Switch module, or use the alternative channels on BL233 / I2C2PC

Beware: Some PCBs are incorrectly printed with 0x50 as address for 8593.

6 Jumpers

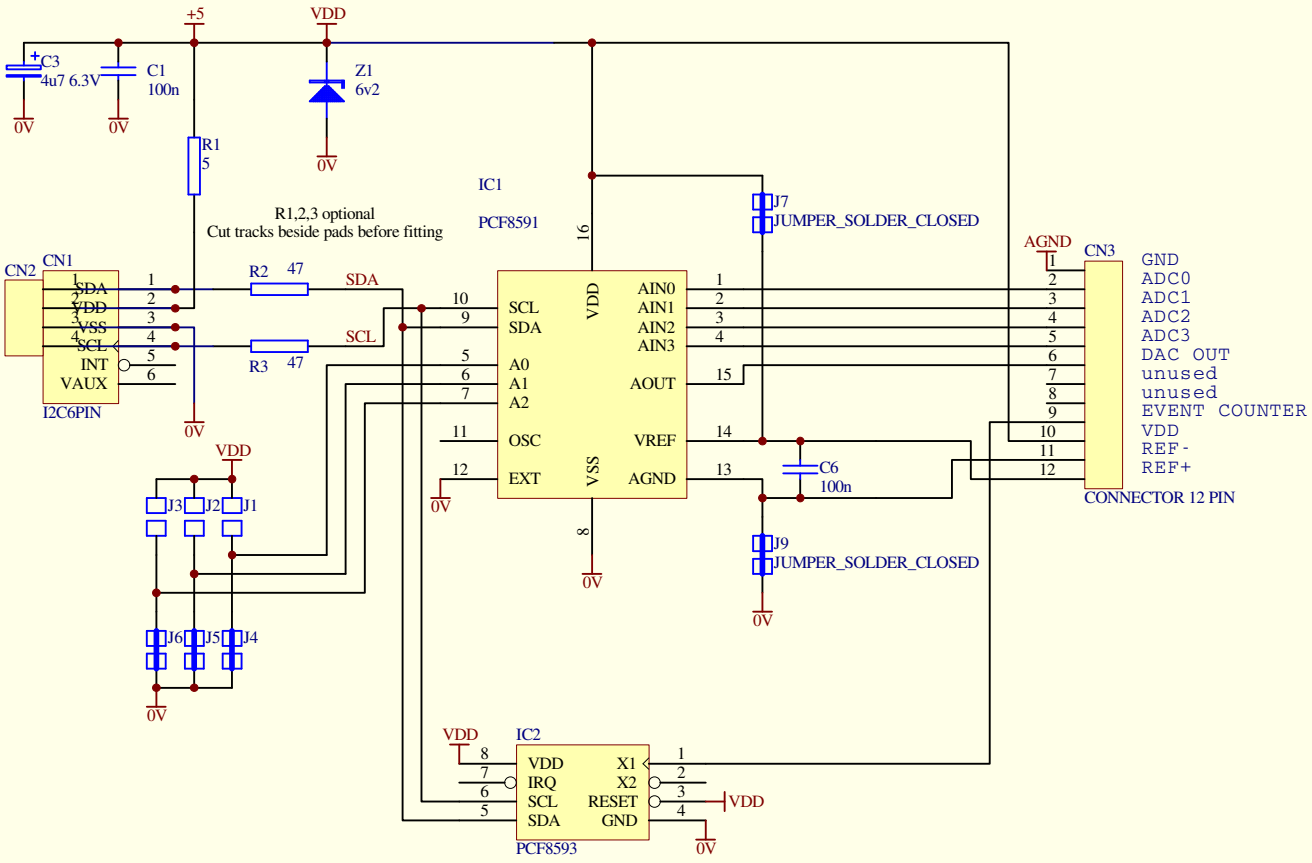
J#	Function	default	
J1-6	I2C Sub Address	joined to 0	
J7	Ref+ to VDD	closed	
J9	Ref- to GND	closed	

7 Edge Connector

Pin	Function	
1	SDA	
2	+5	
3	GND	
4	SCL	
5	AGND	
6	ADC0	
7	ADC1	
8	ADC2	
9	ADC3	
10	DAC OUT	
11		
12		
13	EVENT IN	
14	VDD	
15	REF -	
16	REF +	

8 Drawings

8.1 Circuit Diagram



Jumpers

J1-J6 I2C Address

J7: Cut for ext VREF+
J9: Cut for external VREF-

PCF8591 I2C address 90h
PCF8593 I2C address A2h

PSF8591 is an 8 bit, 4 channel ADC + 1 channel DAC

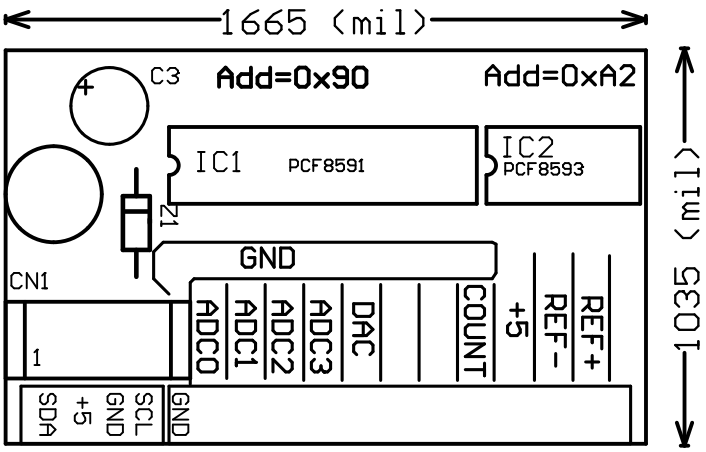
PCF8593 is used as a 6 digit BCD event counter.
Event Counter mode must be selected.
The input can be AC coupled as it has oscillator bias.
Alternatively it can be pulled up or down with a resistor.

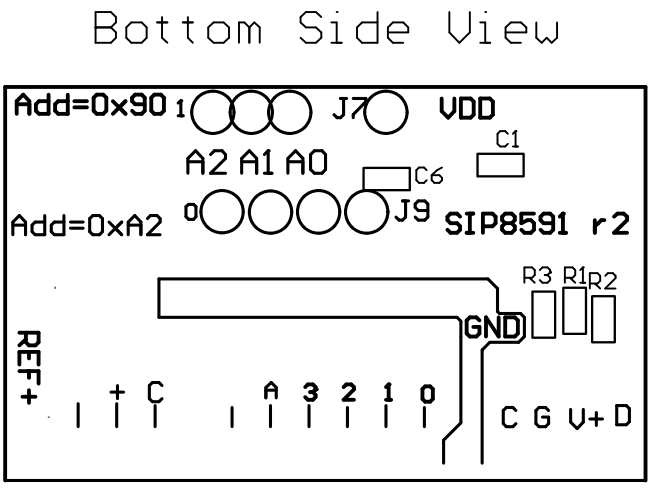
FID2 FIDUCIAL-BOT
FID1 FIDUCIAL-BOT
H1 HOLE-M3
0V
MP1
PCB-SIP8591b

Designed and Manufactured by
Broadcast Equipment Ltd
www.i2cchip.com

Title: **8 Bit ADC/DAC & 6 Digit Event Counter**		
Size: A4	Number:	Revision:
Date: 12-Oct-2008		Sheet of
File: C:\cad\a\I2CAd\I2CAd.ddb		Drawn By:

8.2 PCB Drawings





9 Revision History

Date	Rev#	Changes
	0	pre-release
21 Mar 2012	1	Add sample I2C command for application